Mixed-Signal Implementation of Analog Front-end and ADC for Compressive Sensing

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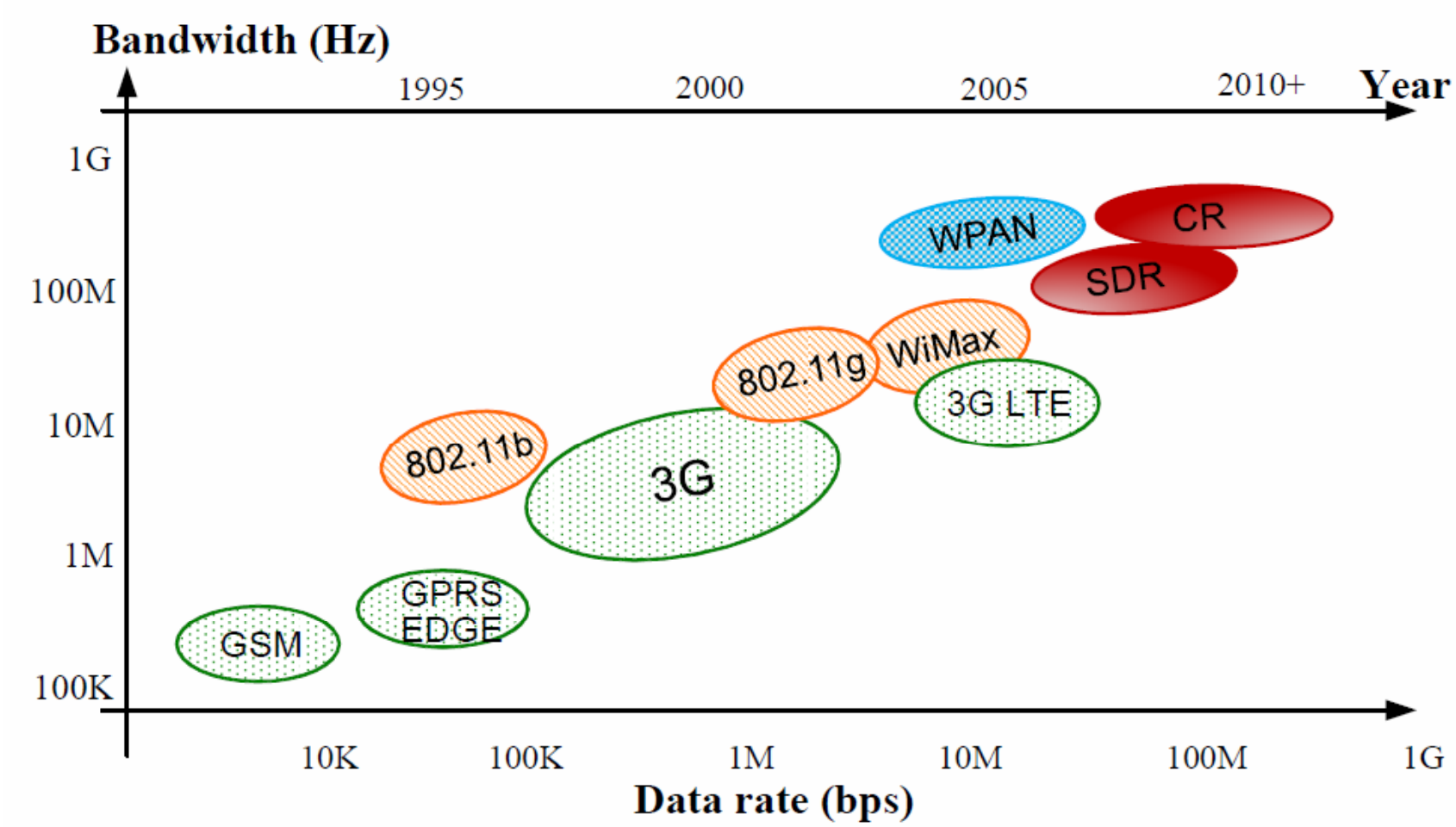
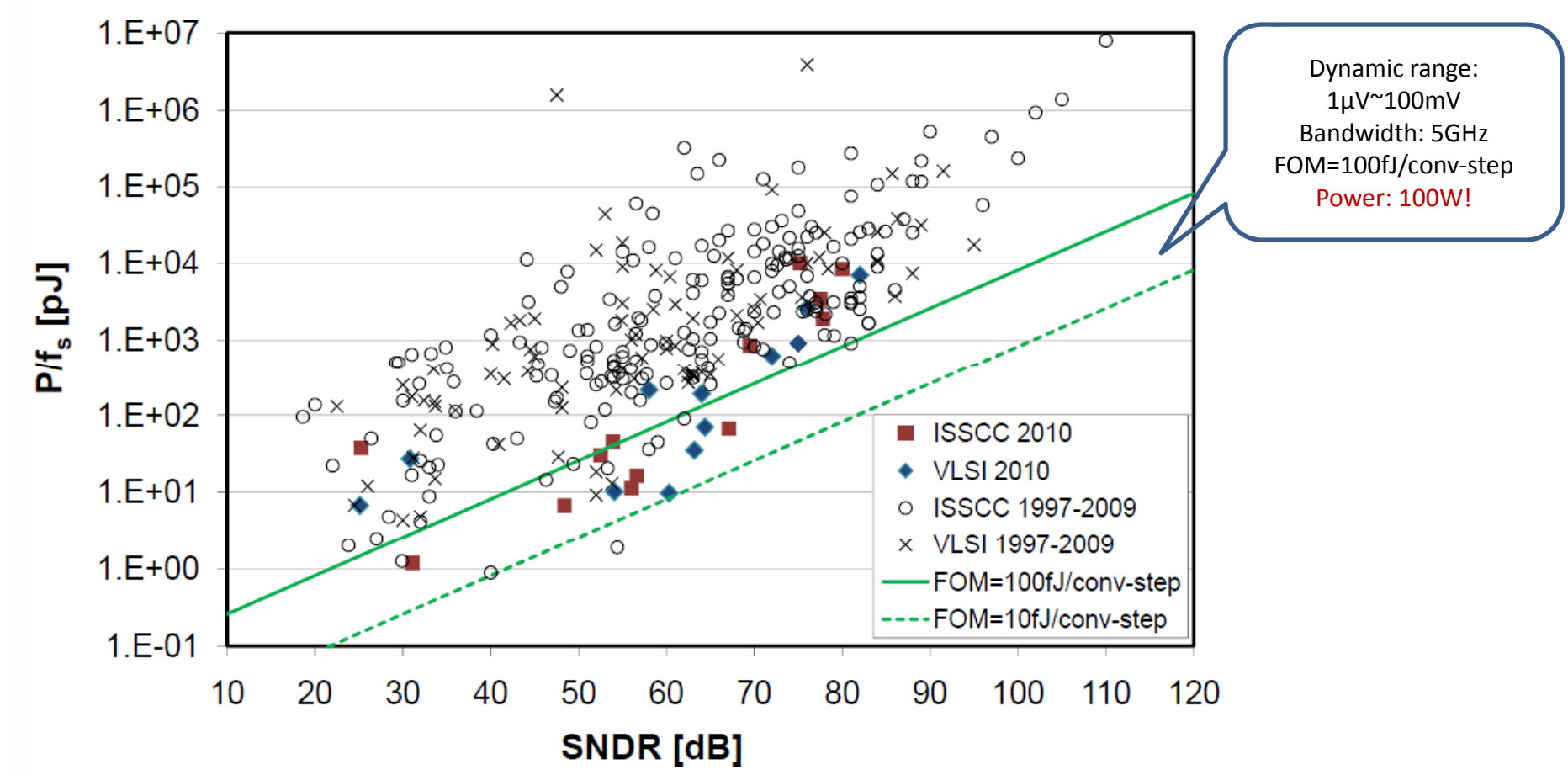
July 6th, 2012

Continuous Bandwidth Growth of Wireless Systems



Energy Consumption of State-of-the-Art ADCs ([1])



Key Question

Is it too conservative to always comply with the Nyquist sampling theory?

Theory of Compressive Sensing (CS) ([3], [4])

- The characteristics of **sparse** signals can be captured at its information rate which is usually much lower than the Nyquist rate.

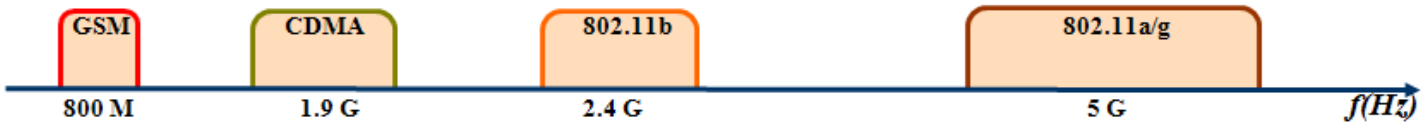
Sparse Signals

- Naturally existed sparse signals
  - Sparse signals

$$r(t) = \sum_{i=0}^{S-1} a_i \Psi_i(t) = \mathbf{\Psi a}$$

$$\text{where, } \|a\|_0 = K << S, \quad \Psi_i(t): \text{signal basis function}, \quad a_i : \text{expansion coefficient}$$

  - Examples
    - Images, videos (wavelet-domain sparse);
    - UWB pulse trainings(time-domain sparse);
    - Frequency usage (frequency-domain sparse) ([2]);

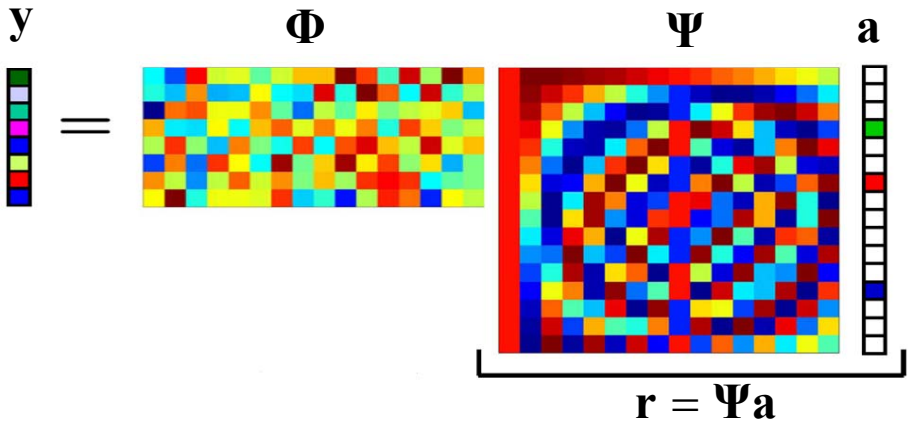


Compressive Sensing

- How CS works?
  - Given a K-sparse vector

$$\mathbf{r} = \mathbf{\Psi a} \qquad \text{where, } \|\mathbf{a}\|_0 = K << S$$

  - Step 1: random projection ([5])



$\mathbf{a}$: expansion coefficients

$\mathbf{\Psi}$: signal basis

$\mathbf{\Phi}$: projection matrix,

$\mathbf{y}$: compressive samples

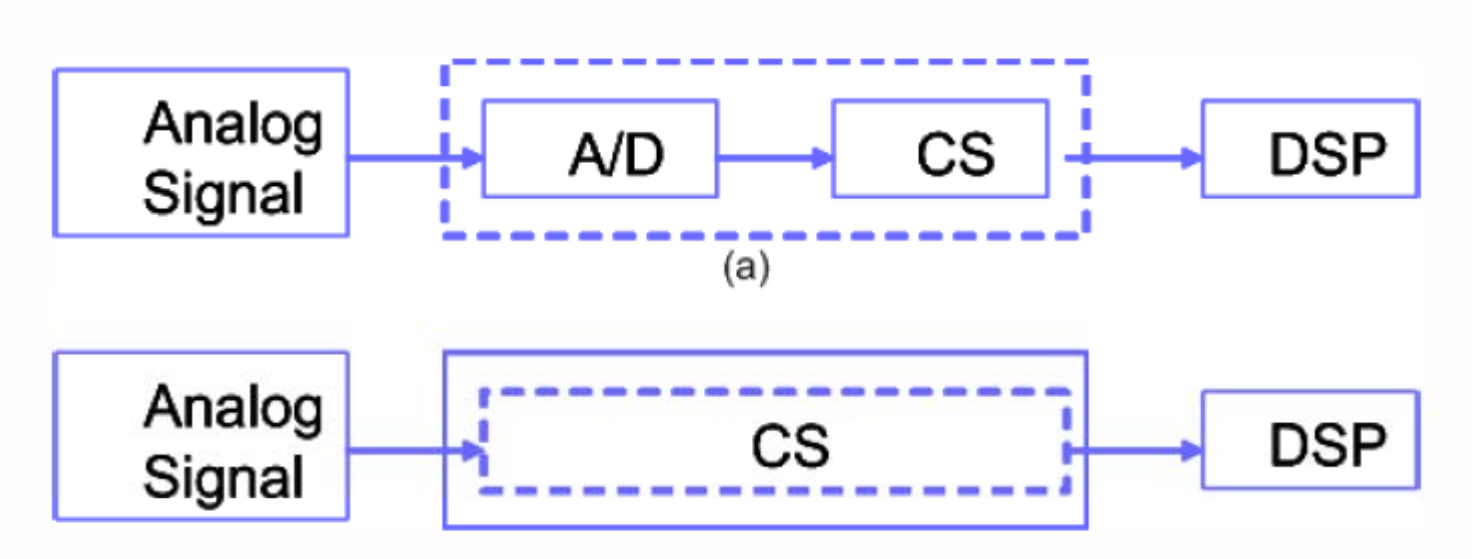
$\mathbf{V}$: reconstruction matrix

  - Step 2: reconstruction

$$\hat{\mathbf{a}} = \text{argmin} \|\mathbf{a}\|_1 \quad \text{s.t.} \quad \mathbf{y} = \mathbf{\Phi\Psi a} = \mathbf{Va}$$

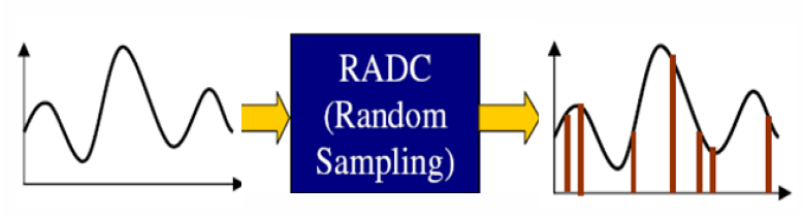
Compressive Sensing of Analog Signals

- CS of digital signals vs. CS of analog signals



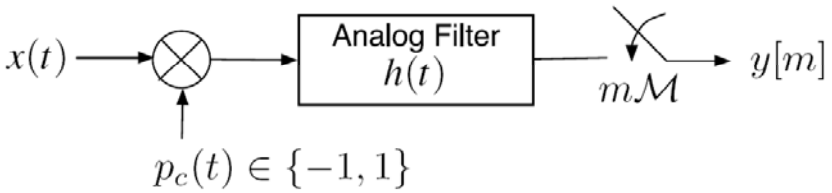
Compressive Sensing of Analog Signals

- Non-uniform sampling ([6])



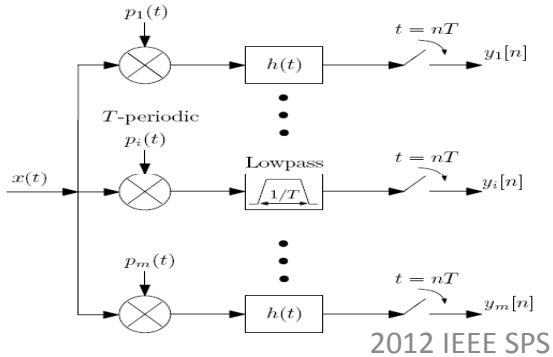
! Difficult to maintain the timing shift accuracy at high-speed.
! Although the average sampling rate is sub-Nyquist, the sampling clock still runs at Nyquist rate.

- Random demodulation ([7])



! Does not consider practical constraints.
! Lacks the flexibility

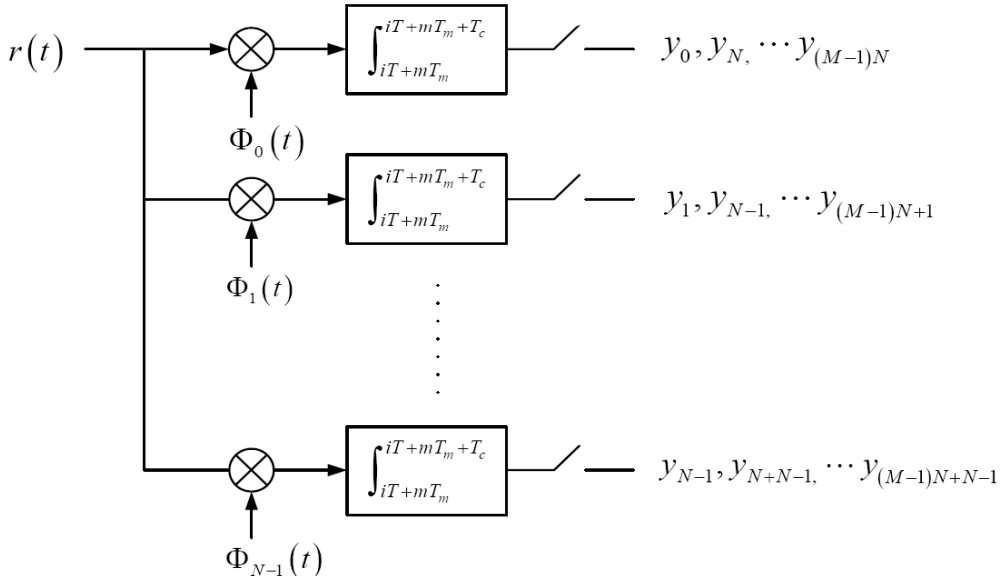
- Modulated Wideband Converter ([8])



! # of channels ≥ 4*# of bands, which is huge in terms of implementation.
! Challenging in generating the T-periodic waveforms.

Parallel Approach

- Parallel Segmented Compressive Sensing (PSCS) front-end

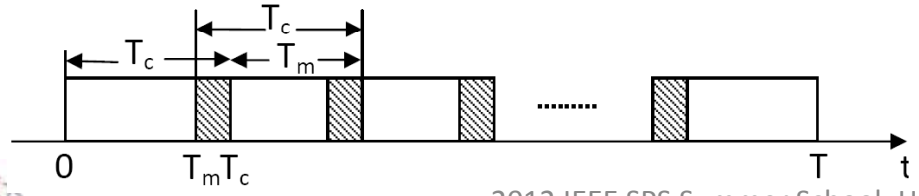


- N: # of parallel paths
- M: # of samples per parallel path
- T_c: integration time
- T_{OVR}: overlapping time
- T_m: T_c-T_{OVR}
- $\Phi_n(t)$: random basis

$$r(t) = \sum_{i=0}^{S-1} a_i \Psi_i(t) + n(t) = \mathbf{\Psi a} + n(t)$$

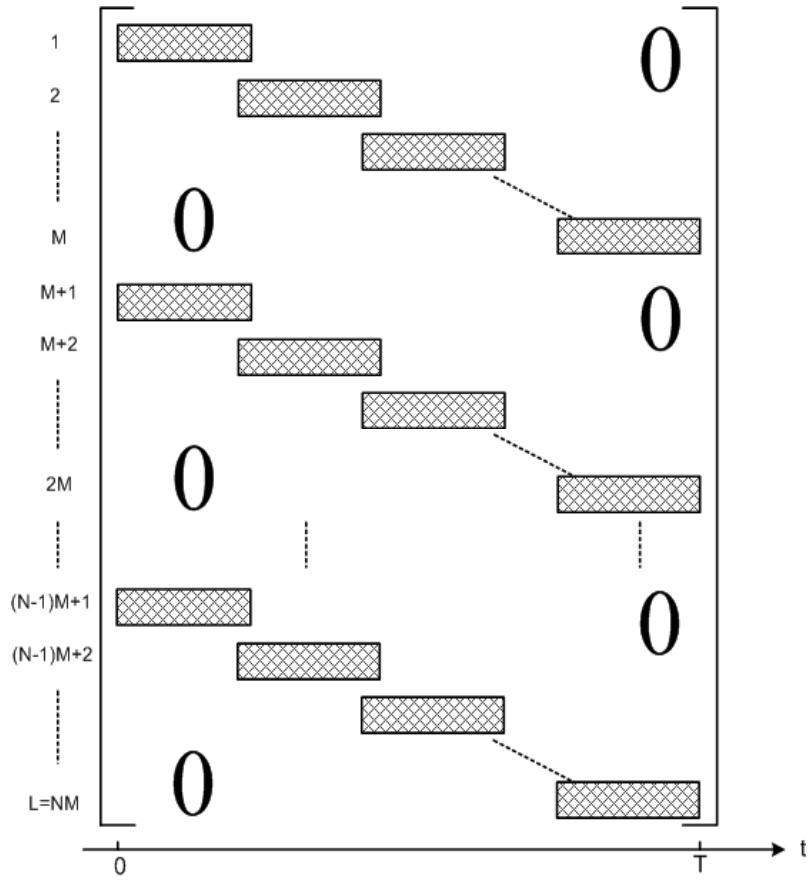
$$y_{mN+n} = \int_{mT_m}^{mT_m+T_c} r(t)\Phi_n^*(t)dt$$

- Overlapping windowing

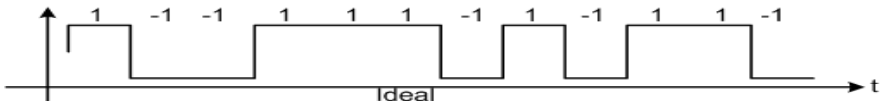


Matrix Representation of Parallel Approach

- **Random projection "matrix"**



- "Mixed-signal" feature;
- Bernoulli distribution (1/-1);

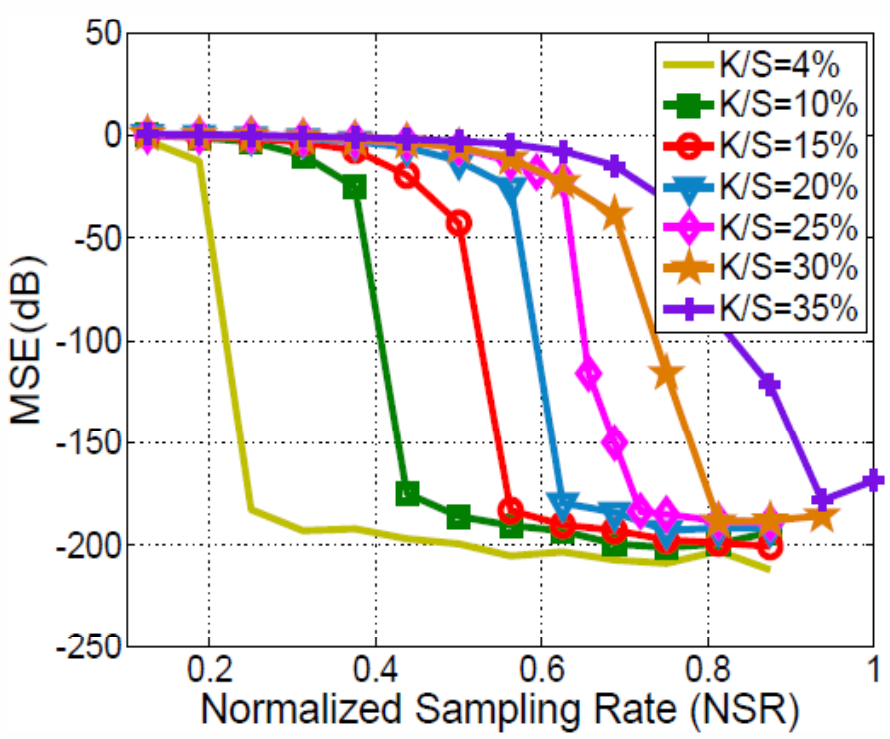


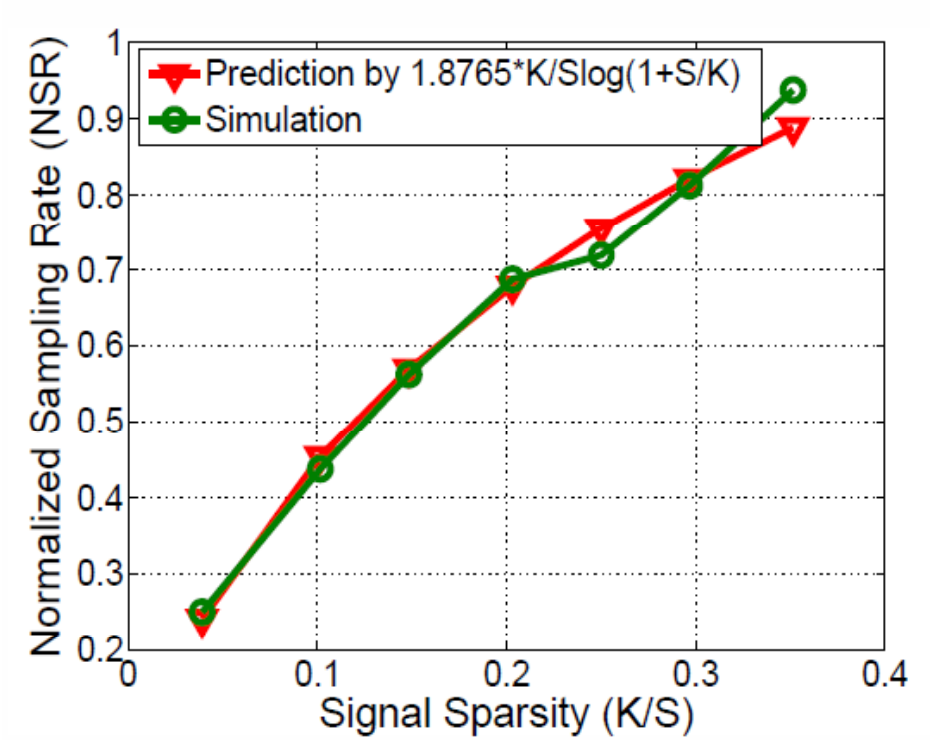
- Each parallel path's basis function is independent.

$$\mathbf{y} = \mathbf{\Phi} * \mathbf{\Psi a}$$

Performance vs. Sampling Rate and Sparsity

- Sub-Nyquist rate sampling and reconstruction

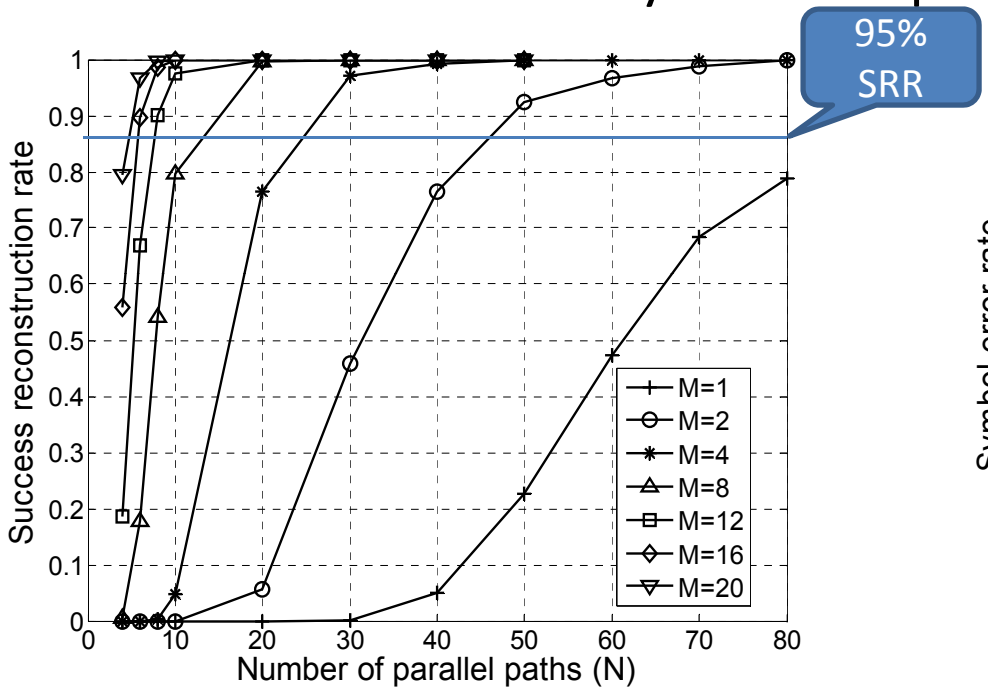


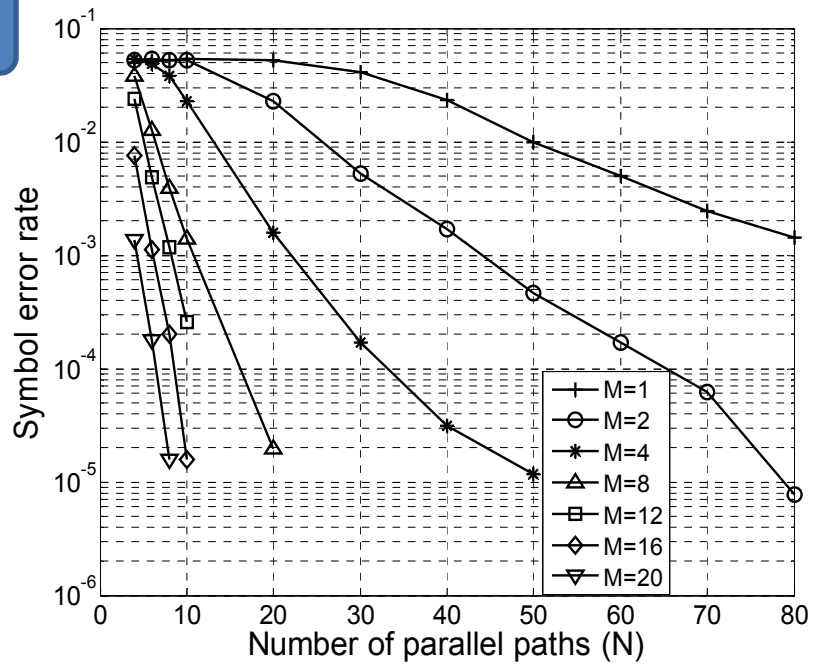


$$MSE = \frac{\|\mathbf{a} - \hat{\mathbf{a}}\|_2^2}{\|\mathbf{a}\|_2^2} \qquad NSR = \frac{f_{Nq}}{f_{CS}} = \frac{MN}{S}$$

Performance vs. Complexity

- Tradeoff between the system complexity and the sampling rate





• Successful Reconstruction Rate (SRR): one *successful reconstruction* is claimed if

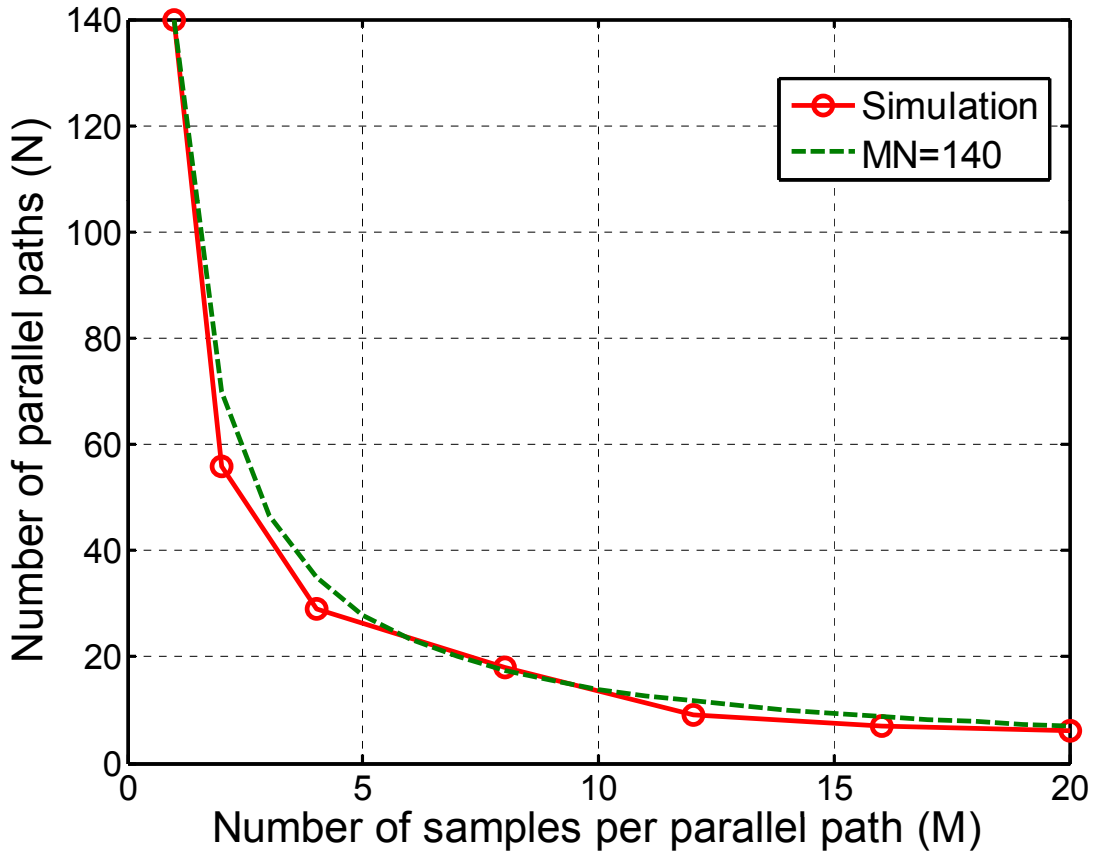
$$\hat{a}_i = a_i, \text{ for all } i$$

• Symbol Error Rate (SER): one *symbol error* at the ith symbol is claimed if $\hat{a}_i \neq a_i$

BW=528MHz, S=256, K=10, SNR=10dB, OMP is used for reconstruction, and a is QPSK modulated.

Complexity vs. Sampling Rate

- Tradeoff between the system complexity and the sampling rate



Obtained by selecting the points corresponding to a Successful Reconstruction Rate=95% in previous simulation results.

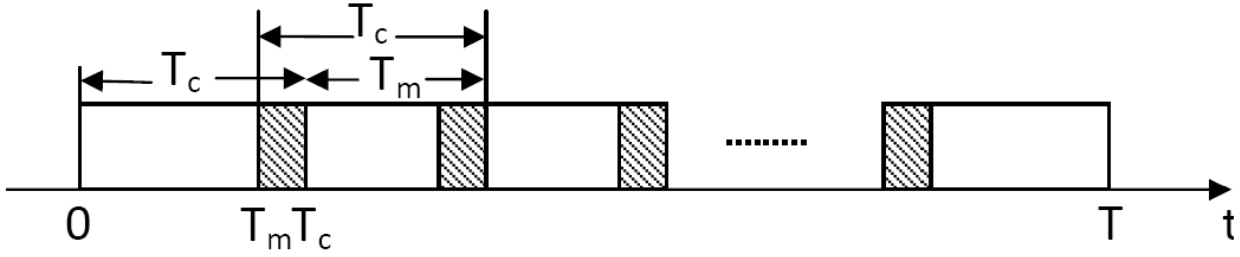
M*N is approximately a constant!

Practical Imperfections

- Spurious frequency components (clock leakage, etc)
- ADC nonlinearity
- Static error (mismatches, offsets, delays, etc) in the PSCS front-end
- Random errors (noise, jitter, etc)

Flexible Spurs Rejection

- Windowed integration acts as low-pass filter with nulls at $k*f_0$, where $f_0=1/T_c$
- For spurs rejection, we need f_{spurs}/f_0=integer

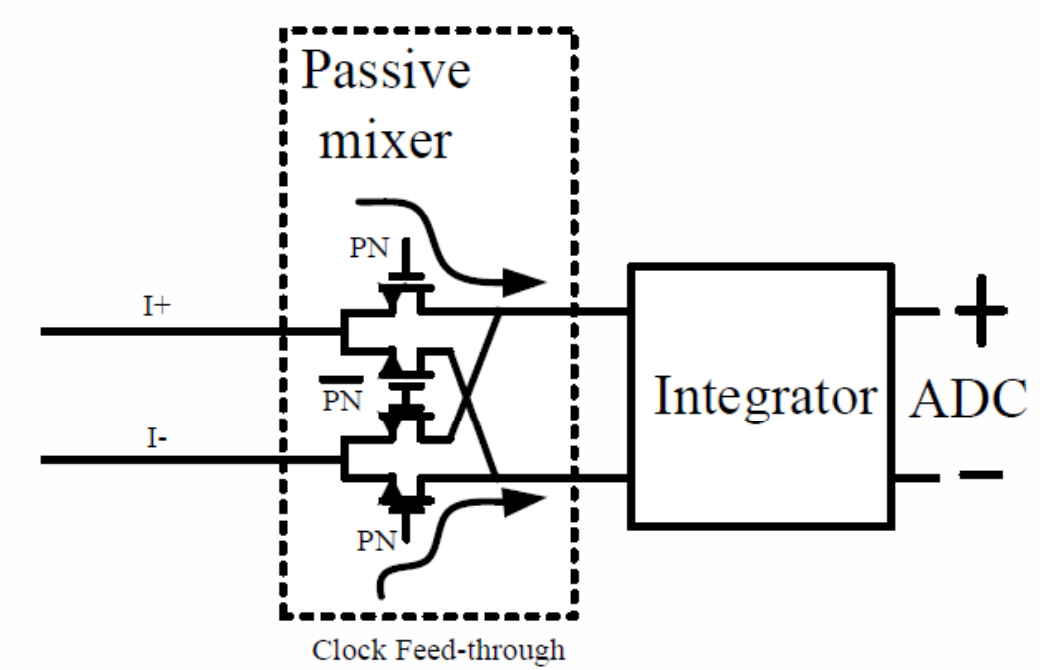


$$OVR = \frac{T_c - T_m}{T_c}$$

$$T = T_c\left(M - (M-1)OVR\right) \quad \Rightarrow \quad \frac{f_{spur}}{f_0} = \frac{f_{spur}\cdot T}{\left(M - (M-1)OVR\right)}$$

Example of Spurious Frequency

- Leakage from the PN clocks to integrators

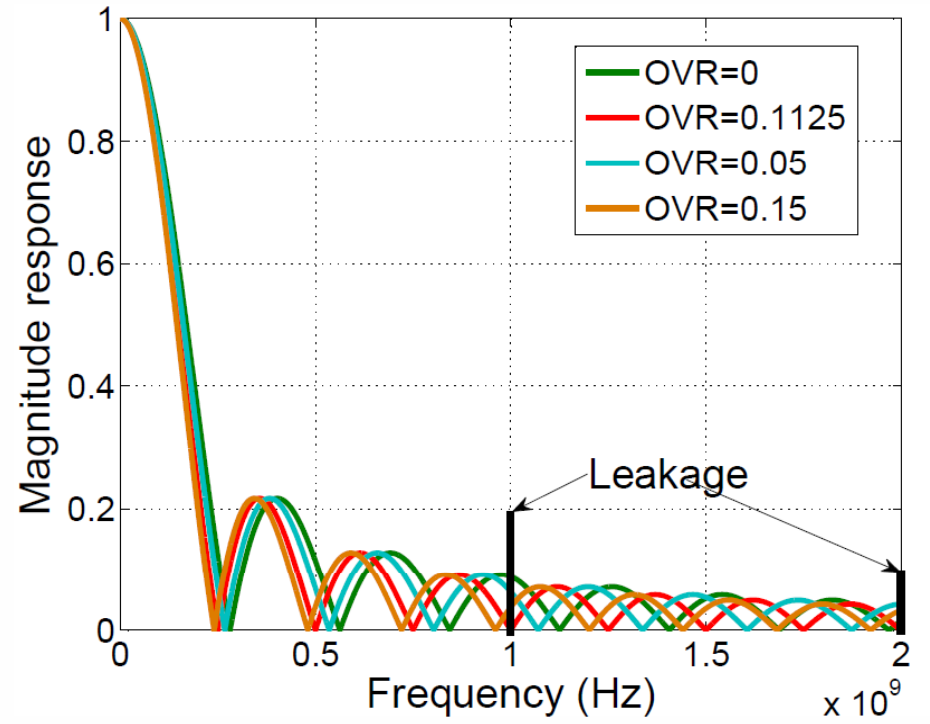


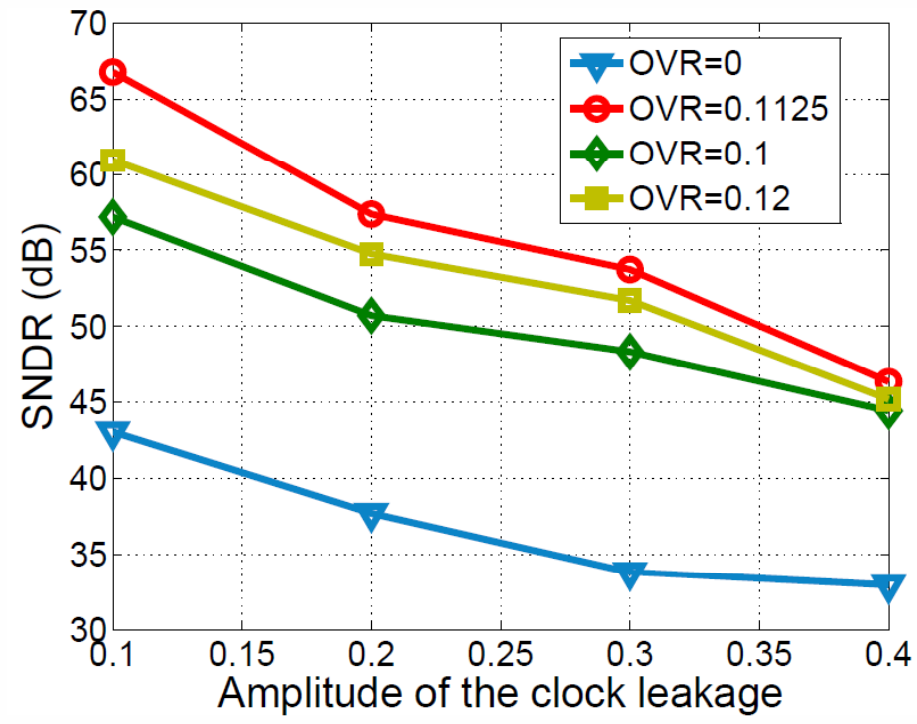
$$\frac{f_{spur}}{f_0} = \frac{f_{spur} \cdot T}{\left(M - (M-1)OVR\right)} \quad \Rightarrow \quad \frac{f_{spur}}{f_0} = \frac{S}{\left(M - (M-1)OVR\right)}$$

$$f_{spur} = f_{CLK} = f_{Nq} = S \cdot \Delta f = S / T$$

Flexible Spurs Rejection

- Tuning the null frequency by changing OVR

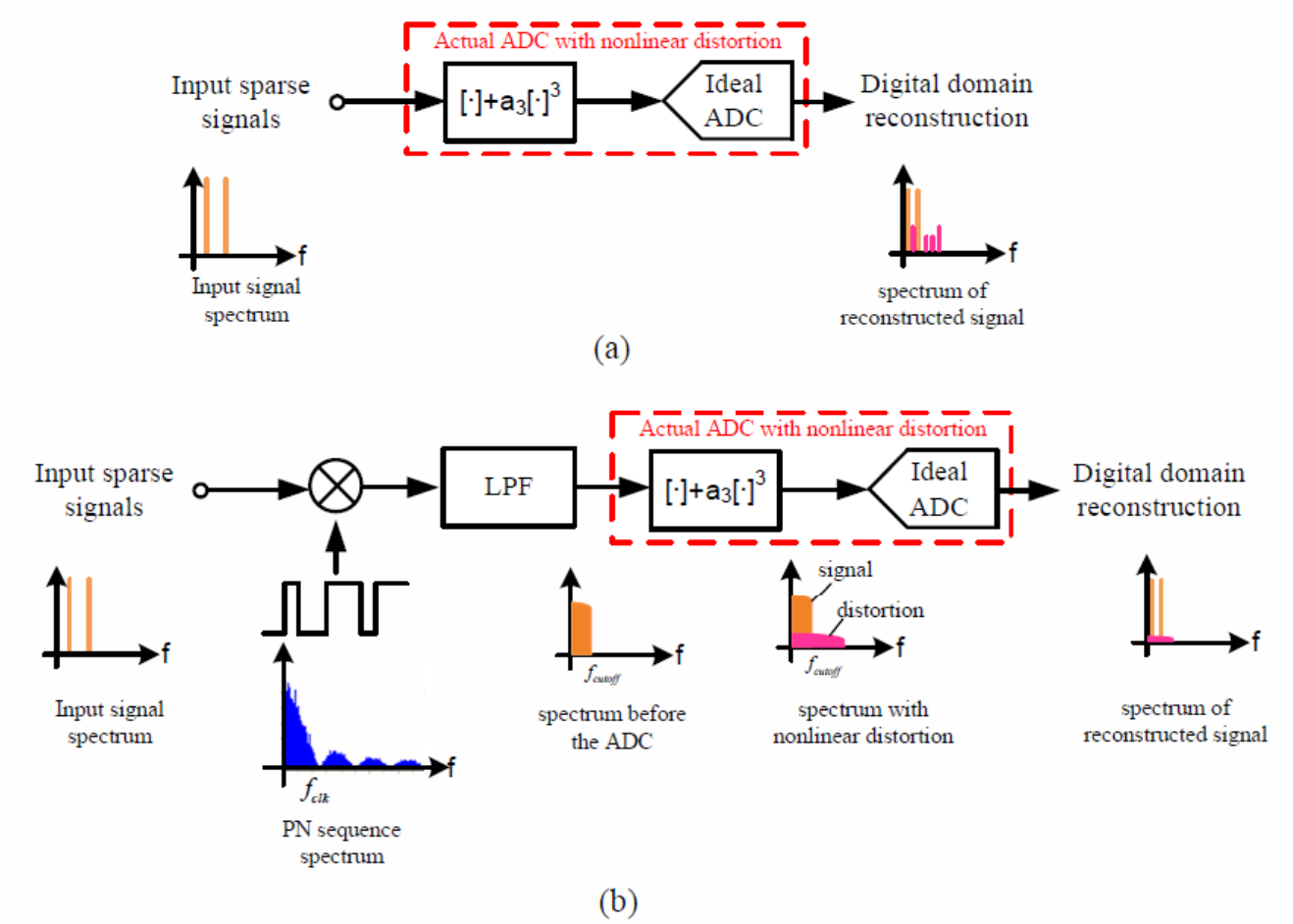




The overlapping windowed integration provides a flexible spurious frequency rejection scheme!

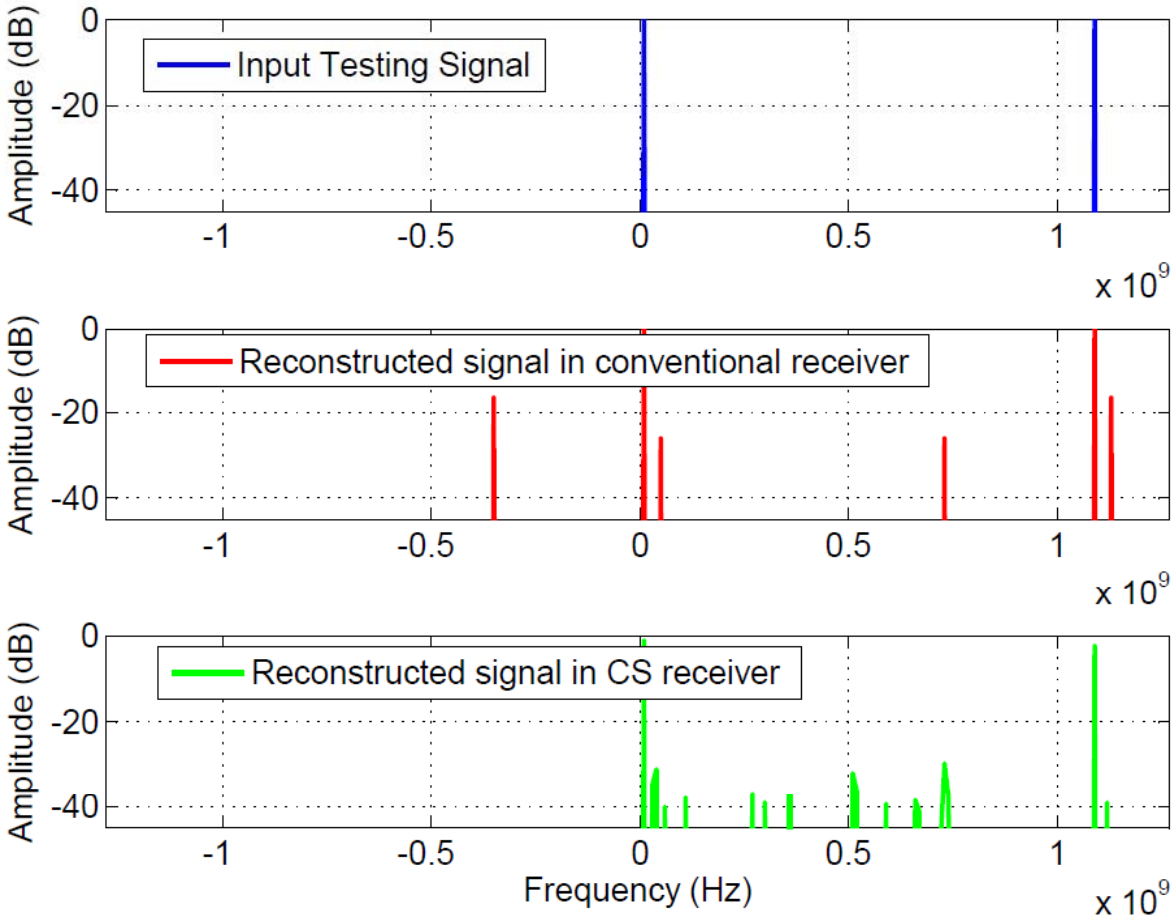
ADC Nonlinearity

- Effect of randomization in the CS system



ADC Nonlinearity

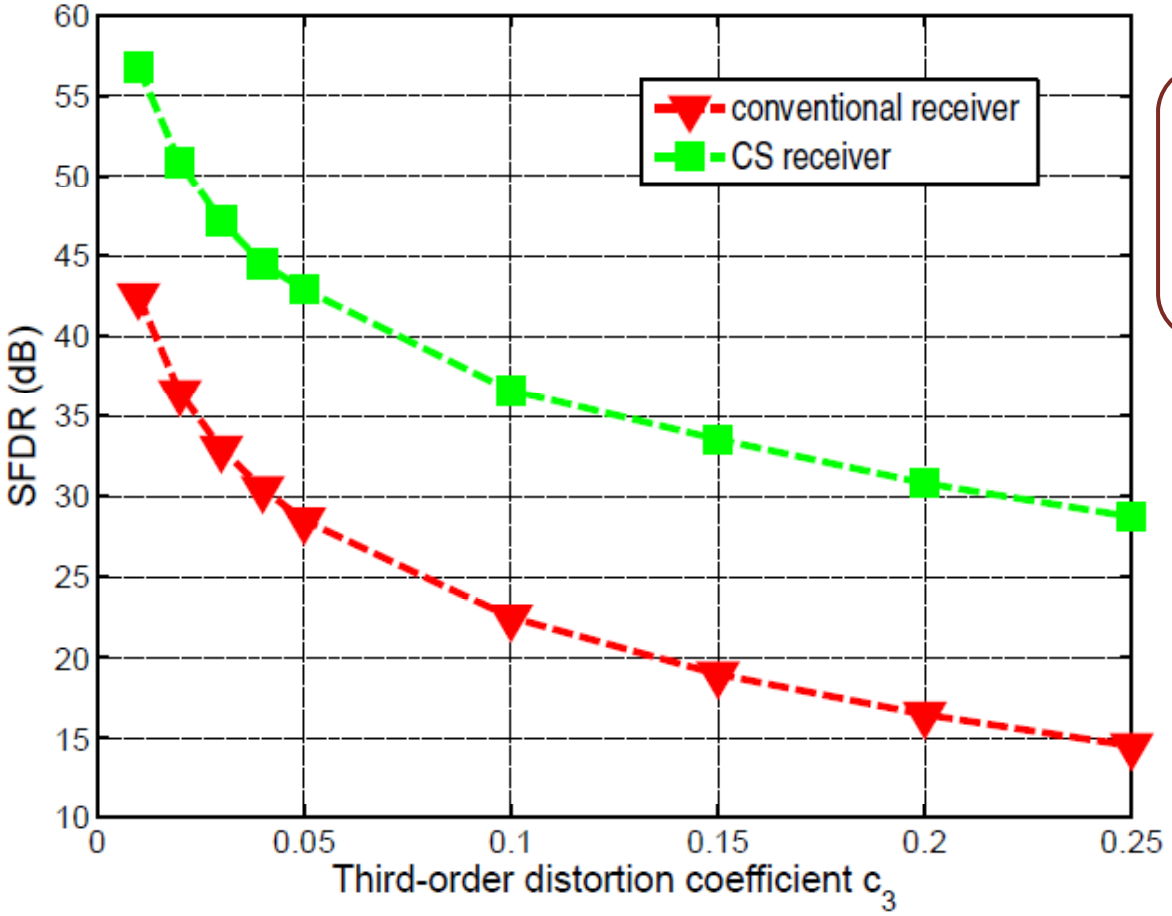
- Two-tone test (noise-free)



- $SFDR_{Nq}$=16.5dB
- $SFDR_{CS}$=29.3dB

ADC nonlinearity

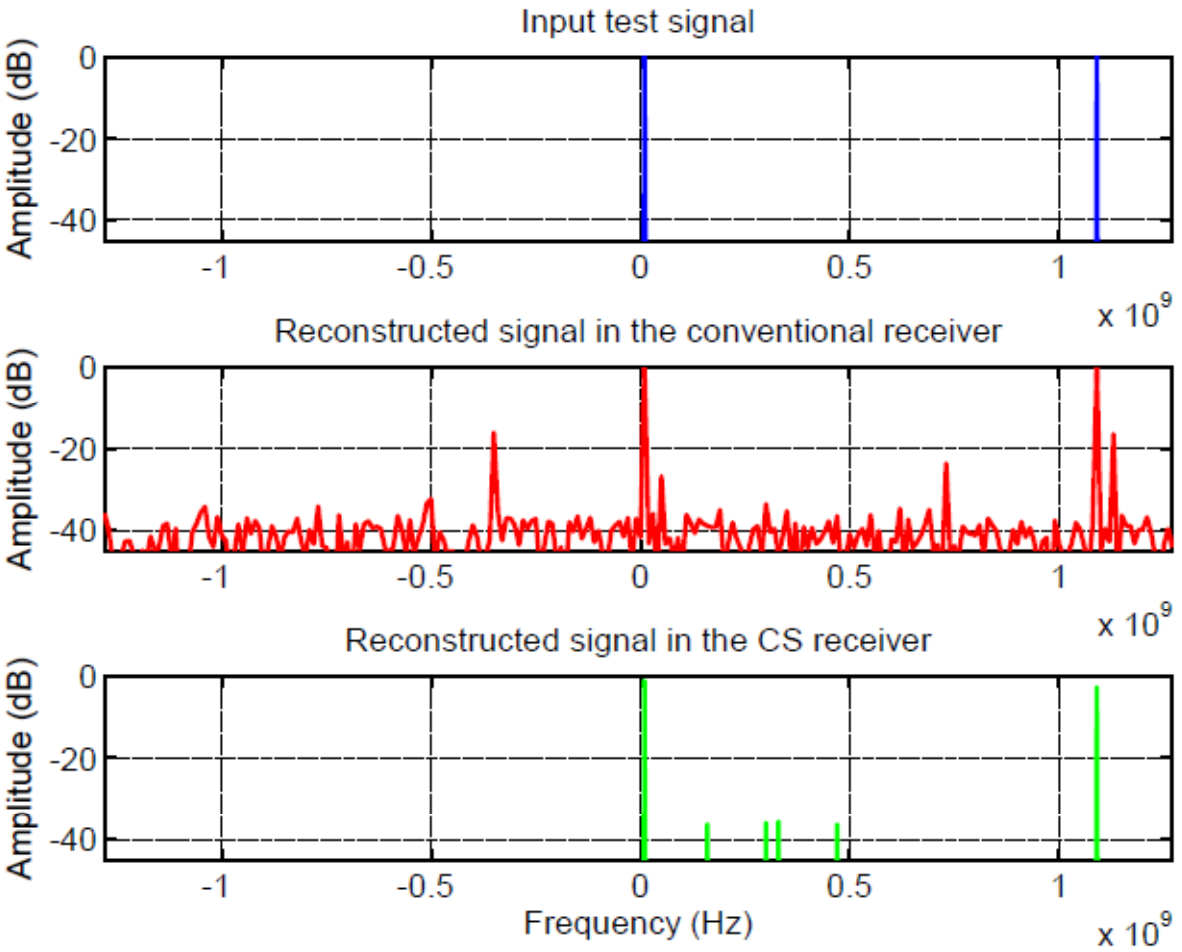
- SFDR improvement from randomization (noise-free)



- 2% sparsity
- Input to ADC: full-scale

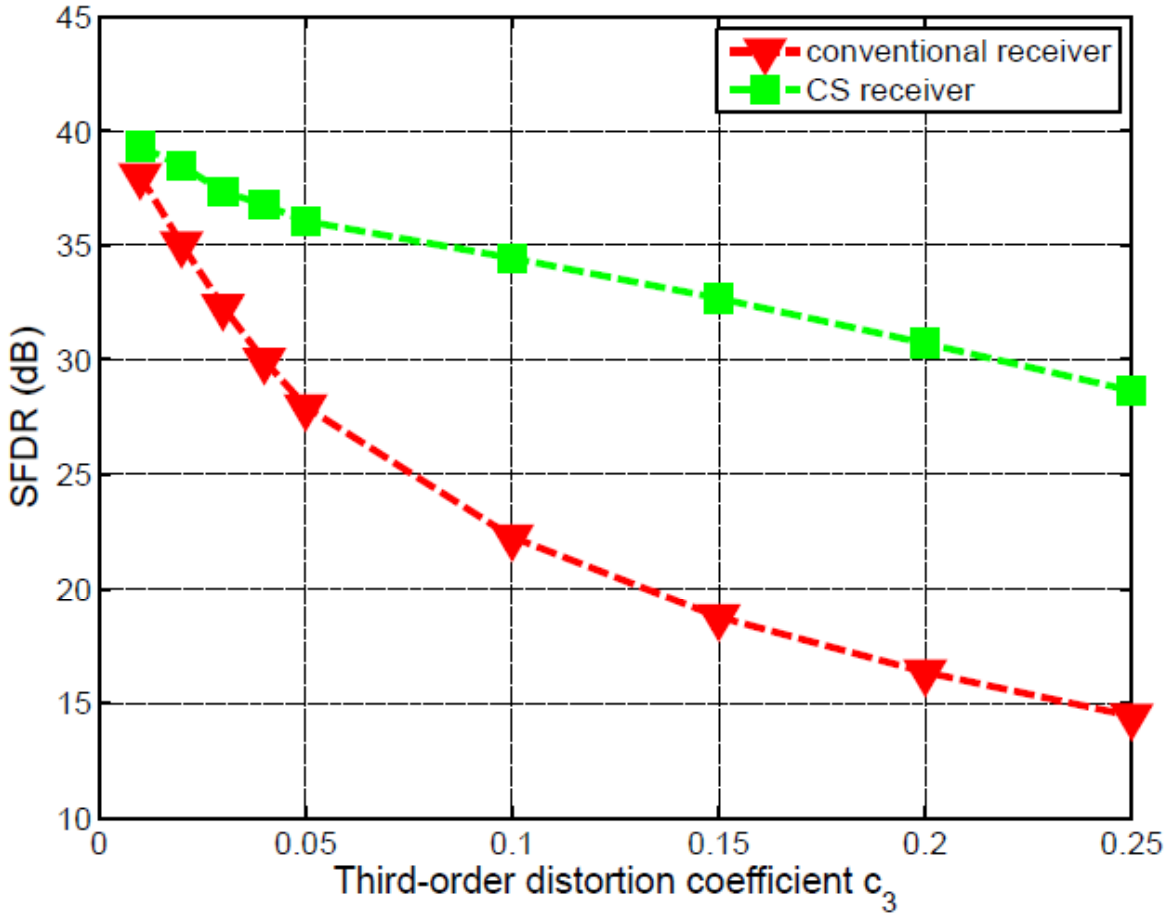
ADC nonlinearity

- Two-tone test (noisy)



ADC nonlinearity

- SFDR improvement from randomization(noisy)



- 2% sparsity
- Input to ADC: full-scale

ADC nonlinearity

- SFDR improvement vs. signal sparsity
  - BW=1.28GHz
  - Input to ADC: full-scale

Sparsity level	2%	4%	10%
CS sampling rate (MHz)	240	480	1200
Median $SFDR_{Nyquist}$ (dB)	42.50	48.13	51.47
Median $SFDR_{CS}$ (dB)	56.80	55.58	53.60
SFDR improvement (dB)	14.30	7.45	2.13

The CS randomization spreads the error power along the signal bandwidth and leads to ADC SFDR improvement!

Static Errors in the PSCS Front-end

- The reconstruction matrix $\mathbf{V}_{MN\times S} = \Phi\Psi$ where
  - Ideally, $V_{(n-1)M+m,i} = \int_{mT_m}^{mT_m+T_c} e^{j2\pi f_i t}\Phi_n(t)dt$
  - Actually, $\int_{mT_m+\delta t_1}^{mT_m+T_c+\delta t_2} \alpha e^{j2\pi(s\Delta f+\delta f)t+\theta}\left(\Phi_n(t)+\delta\Phi_n(t)\right)^* dt = V_{(n-1)M+m,i} + \Delta V_{(n-1)M+m,i}$

- Assuming that the system is linear and time-invariant, given the nominal input $r(t) = \sum_{i=0}^{S-1} a_s e^{j2\pi f_i t} = \mathbf{\Phi a}$
  - The ideal output

    $$\mathbf{y} = \mathbf{Va}$$

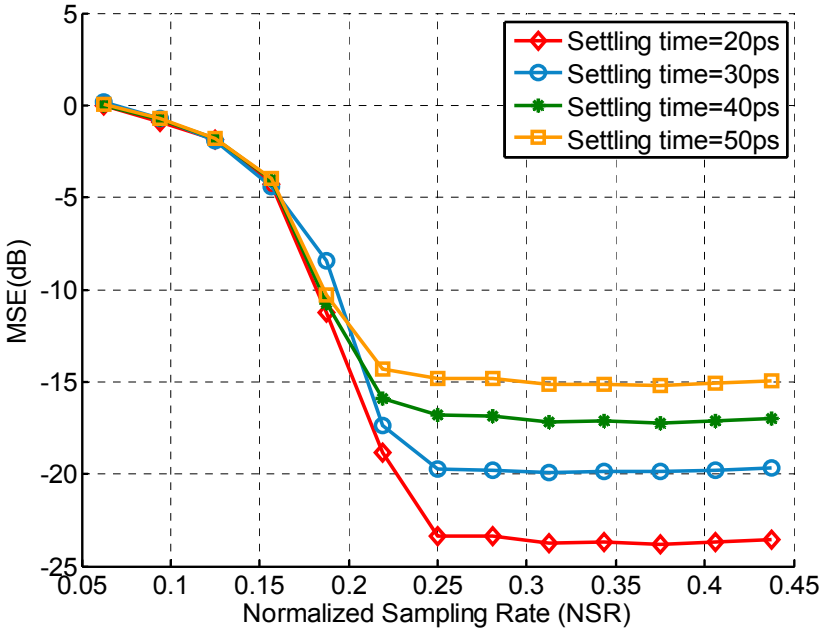
  - The actual output

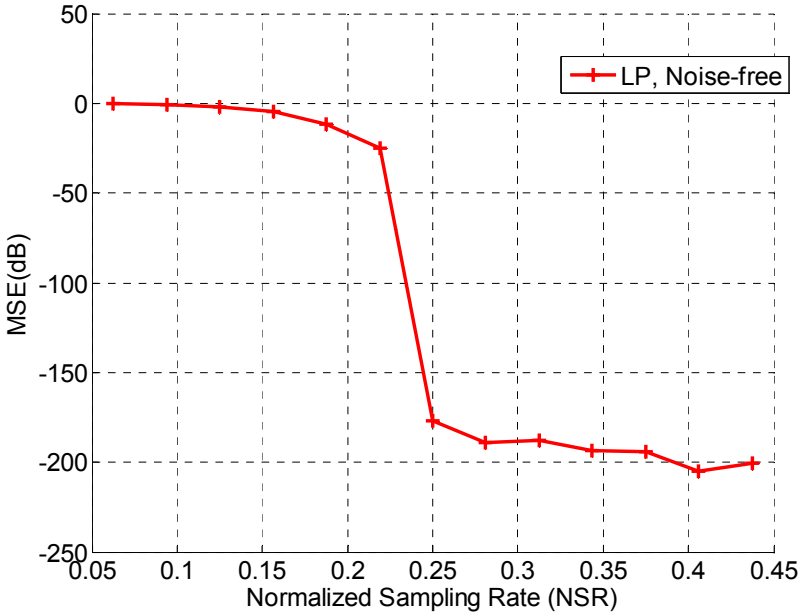
    $$\mathbf{y} = (\mathbf{V} + \Delta\mathbf{V})\mathbf{a}$$

Example of static errors in the PSCS front-end

- Finite settling time of the PN sequences

Ideal case

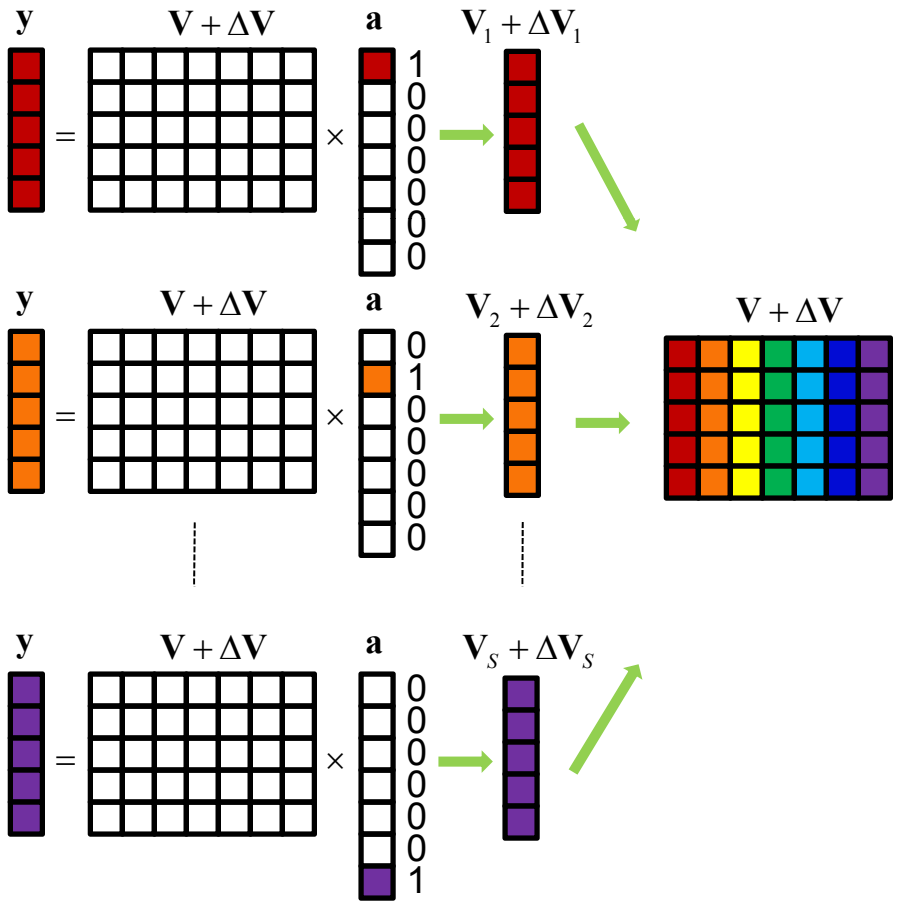




PN sequences have finite settling time.

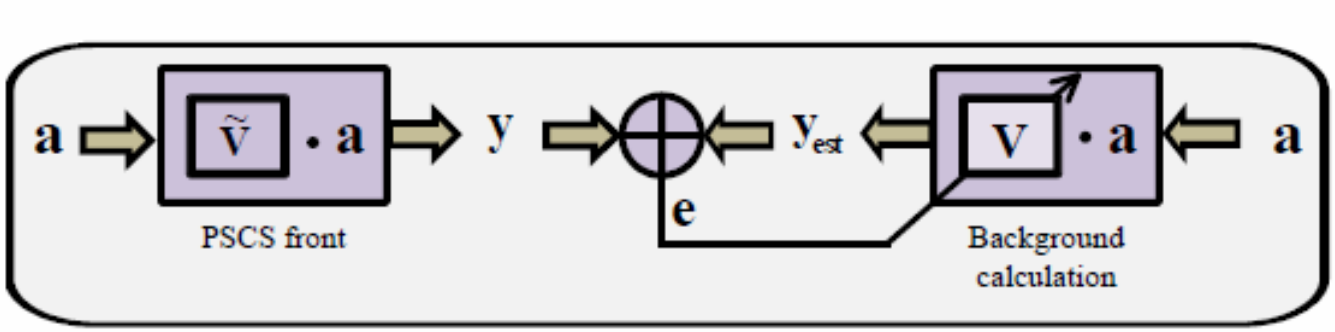
Compensation of Static Errors

- Direct training



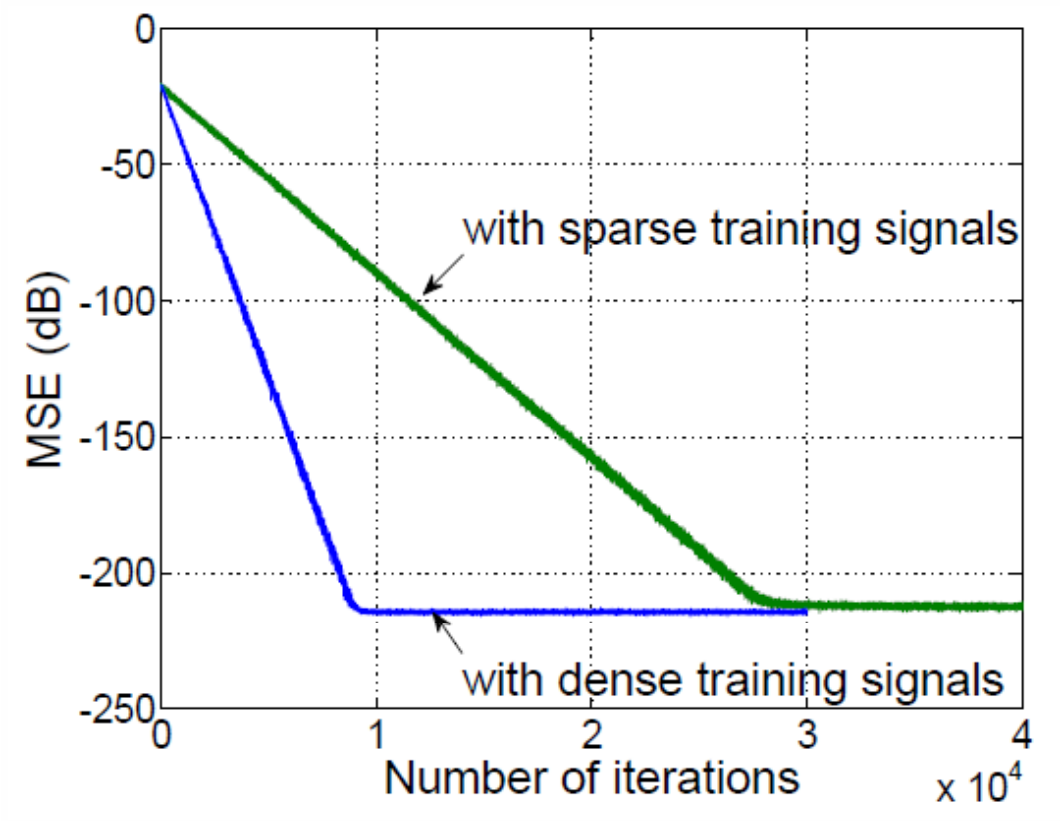
LMS Algorithm for Digital Calibration

- Background iterative calibration



Calibration Results

- Background iterative calibration

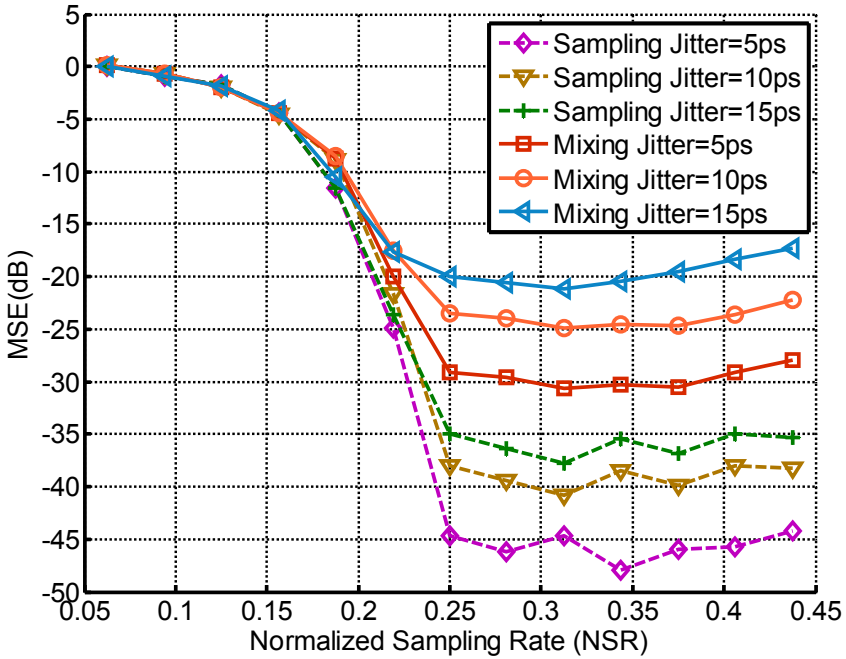


Static errors can be compensated through training and iterative background calibration!

Example of Random Errors in the PSCS front-end

- Noise $\left\|\mathbf{a}-\hat{\mathbf{a}}\right\|_2 \le c\varepsilon_n$ where, $\varepsilon_n = \left\|n\right\|_2$
- Jitter $\mathrm{SNR_j} = \dfrac{V_{sig,output}^{\ 2}}{N_j^{\ 2}} = \dfrac{\lambda}{2\sigma_j^2 f_{clk}^{\ 2}}.$

where, f_{clk} is the clock frequency, σ_j is the std of random jitter, λ depends on the signal characteristics.



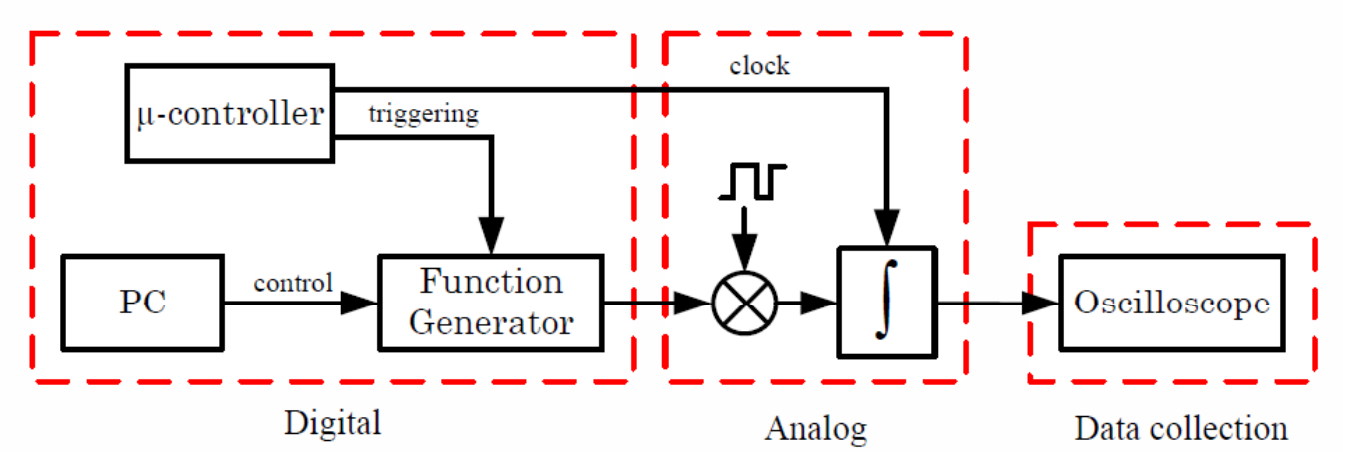
! Random errors can not be calibrated out and need to be paid special attention during circuit-level design.

Low-Frequency Prototype with off-the-Shelf Components

- Design specifications

S	Δf	BW	T=1/Δf	M	N	Δt=T/M	fs=1/Δt	Tc	Tov	OVR
100	2KHz	200KHz	500μs	16	4	31.25 μs	32KHz	36.5 μs	5.6μs	15.34%

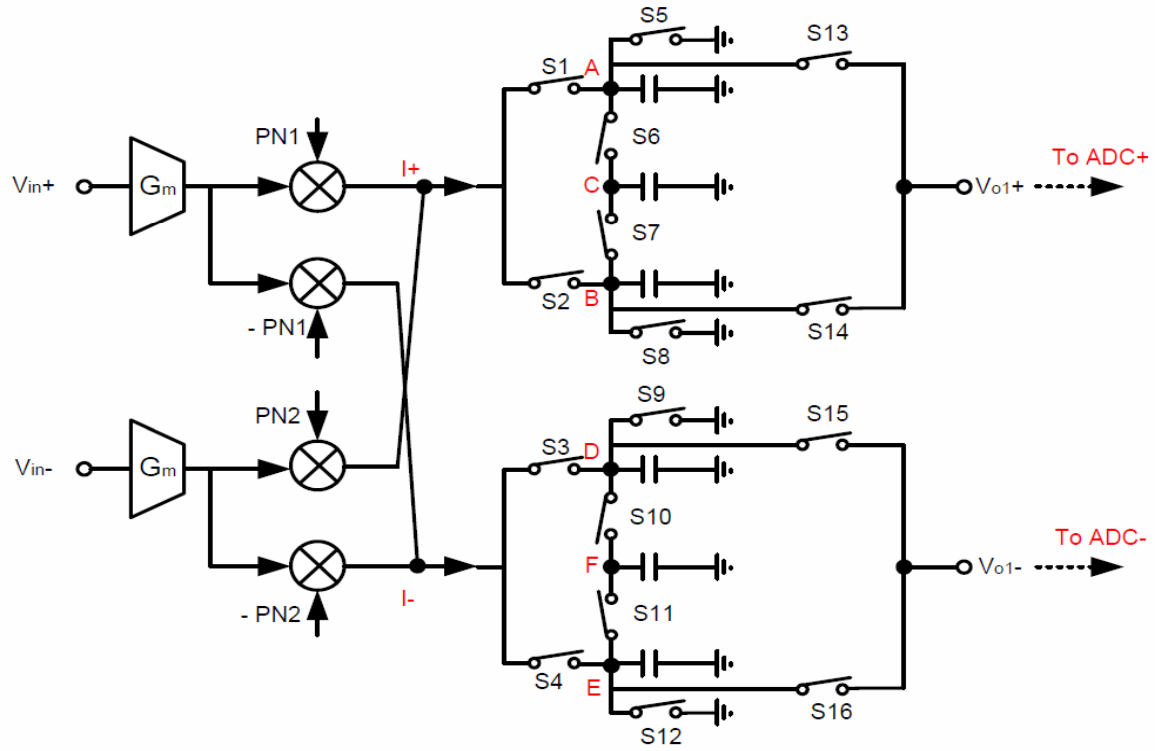
- Overall configuration



- Multi-carrier signal generator
  - Agilent 33120A

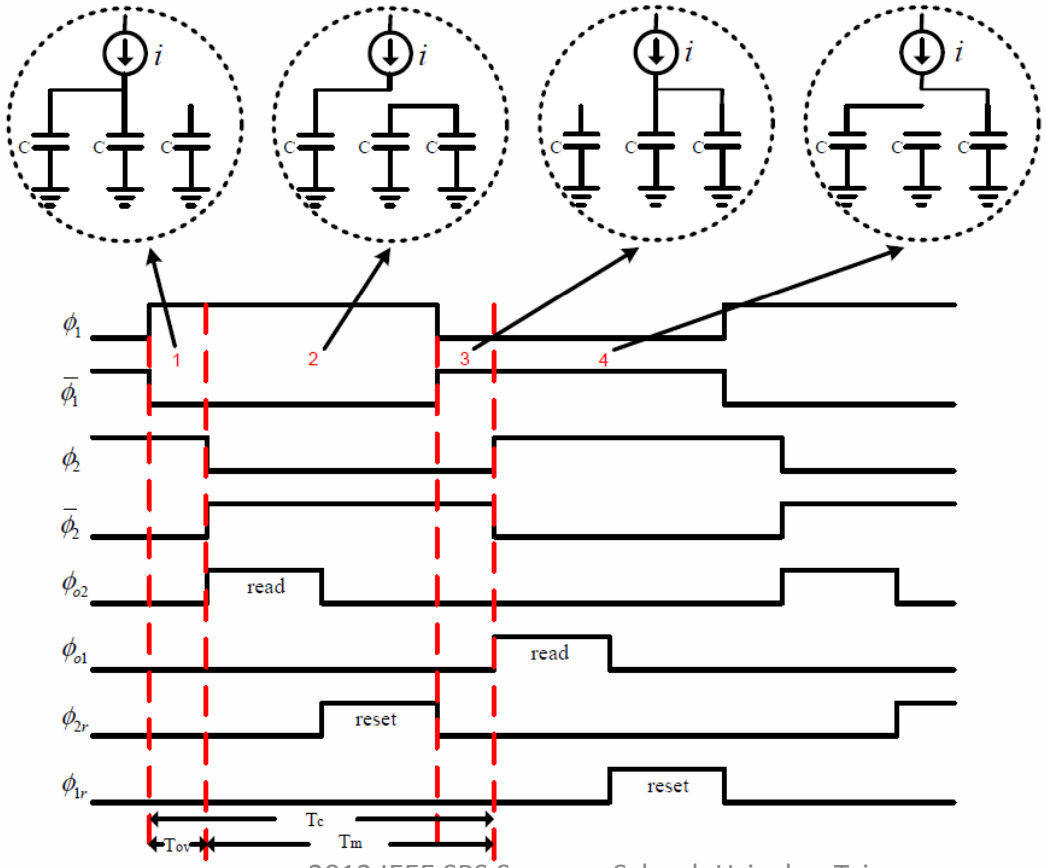
Low-Frequency Prototype with off-the-Shelf Components

- Mixer and Integrators
  - Gm stage: TIOPA861 (Gm=116mS)
  - Switches: CD4066BCN transmission gate



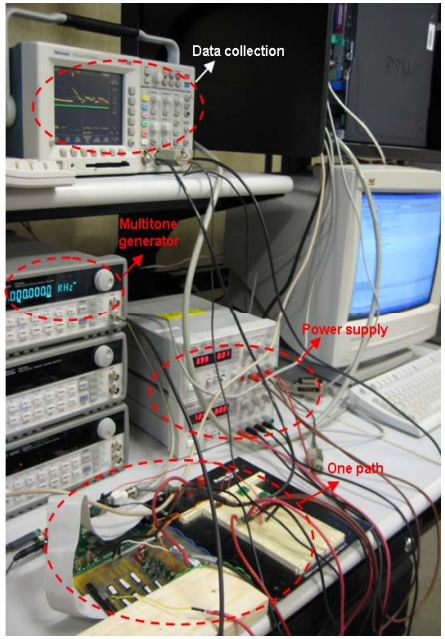
Low-Frequency Prototype with off-the-Shelf Components

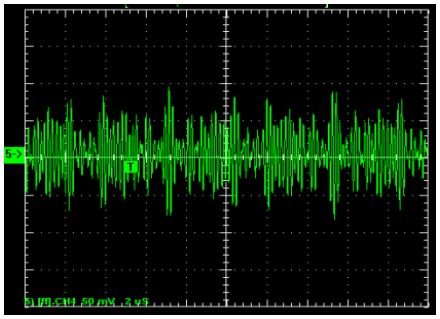
- Mixer and Integrators (cont.)
  - Interleaved integration with overlapping windowing

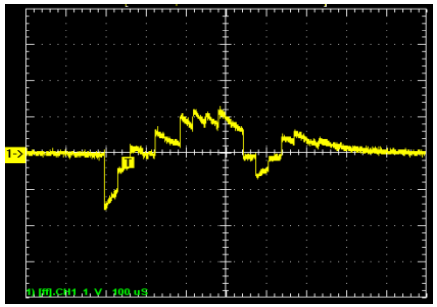


Low-Frequency Prototype with off-the-Shelf Components

- Test setup and Measurement results



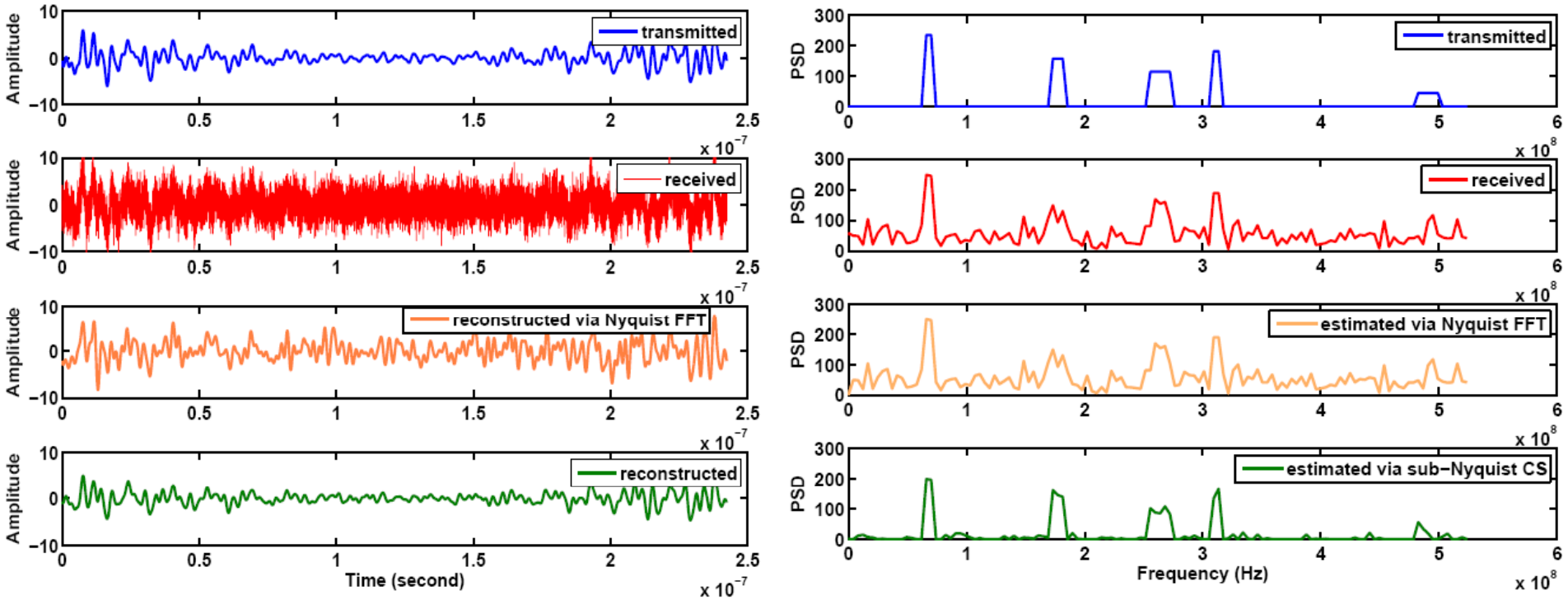




Sub-carrier's amplitude (mV)	Input Testing signal frequency (kHz)	Reconstructed signal's frequency (kHz)
0.3	[61, 121]	[61, 121]
0.3	[41, 131]	[41, 131]
0.3	[41, -131]	[41, -131]
0.3	[-51, 63, 111]	[-51, 63, 111]
0.2	[71, -85, 91, -101]	[71, -85, 91, -101]
0.2	[41, 61, 85, 91, 101]	[41, 85, 91]

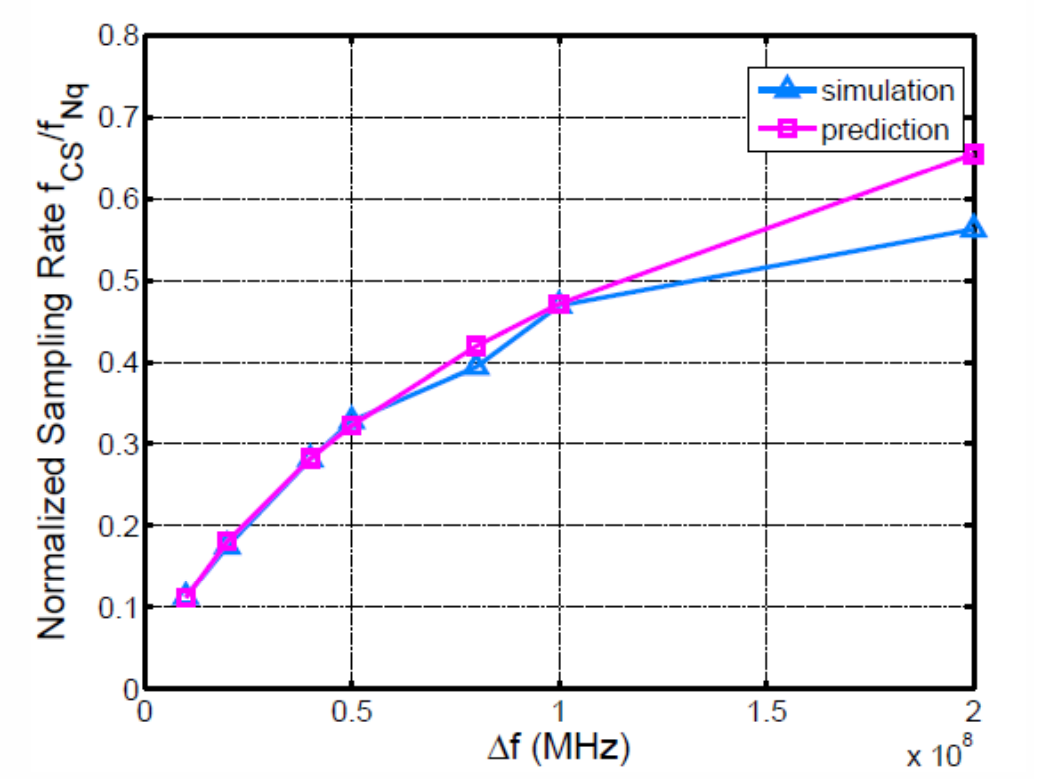
Spectrum Sensing for Cognitive Radios

- Current frequency usage shows some sparsity.
- Simulation setup: S=128, K=17, $SNR_{overall}$=-10dB, NSR=0.32 when PSCS is used.
- Results: MSE=-5dB when Nyquist rate FFT is used, MSE=-14dB when PSCS is used



Digital Spectrum Analyzers

- Ex: THD (Total Harmonic Distortion) test for a DTV receiver.
  - f1=400MHz, up to 5th order harmonics needs to be tested.

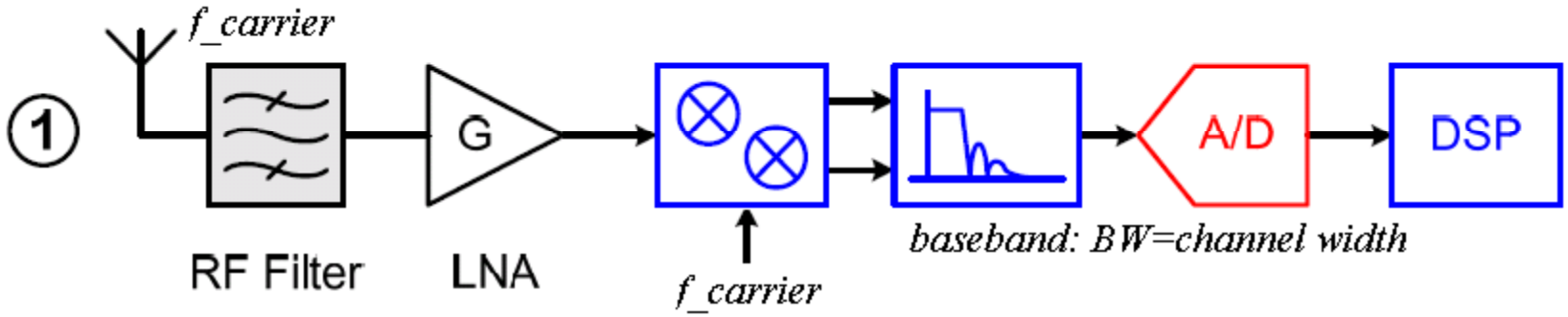


Note that when Δf=10MHz, NSR<0.1, which means that the PSCS front-end (4 path * 100MHz) can work properly to measure the THD at k*400MHz, k=1,2,3,4,5).

$$NSR = c\frac{K\log(1+S/K)}{S} = c\frac{K\Delta f\log\left(1+BW/\left(K\Delta f\right)\right)}{BW}$$

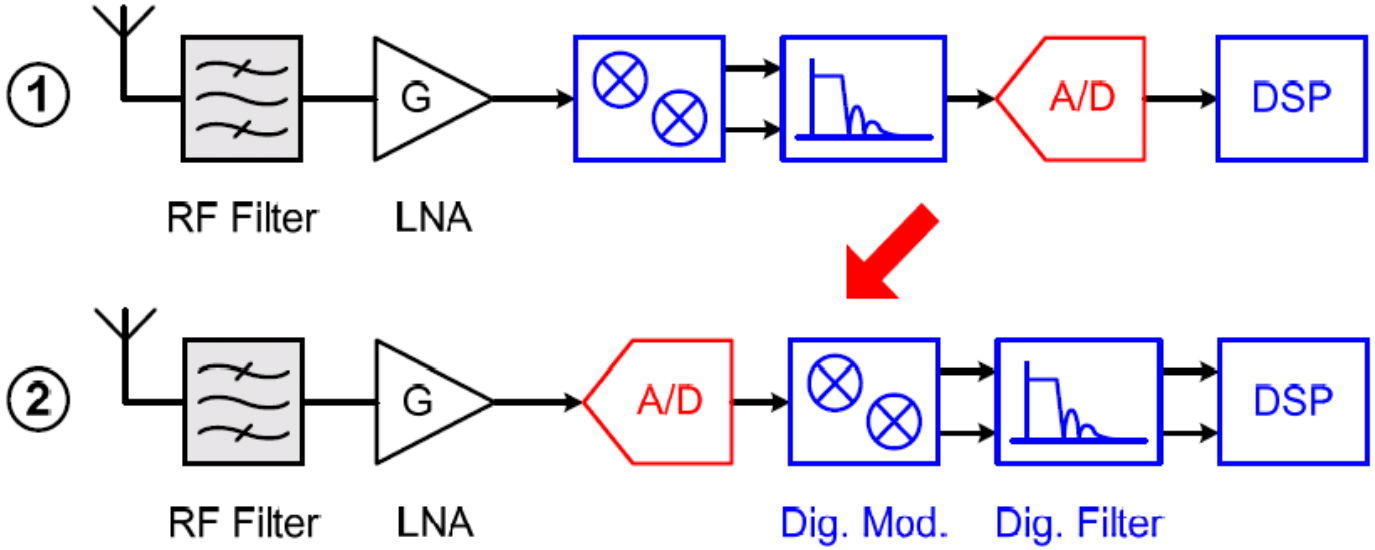
Can CS Really Lower the Sampling Rate of ADCs? At What Cost?

- Traditional RF data acquisition receiver



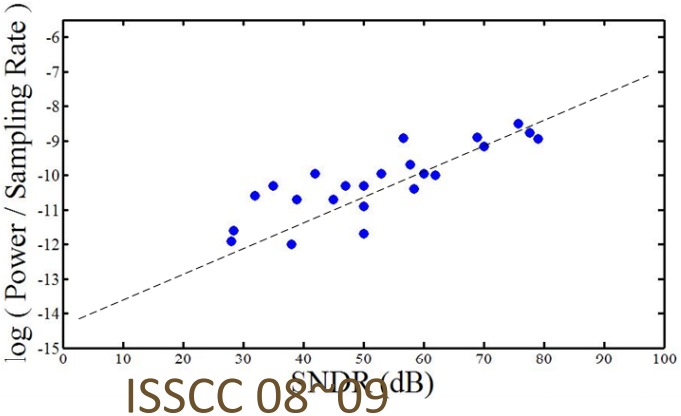
ADC location in RX Chain

- New wideband Application (i.e., Cognitive Radio) Call for high speed & high resolution ADCs

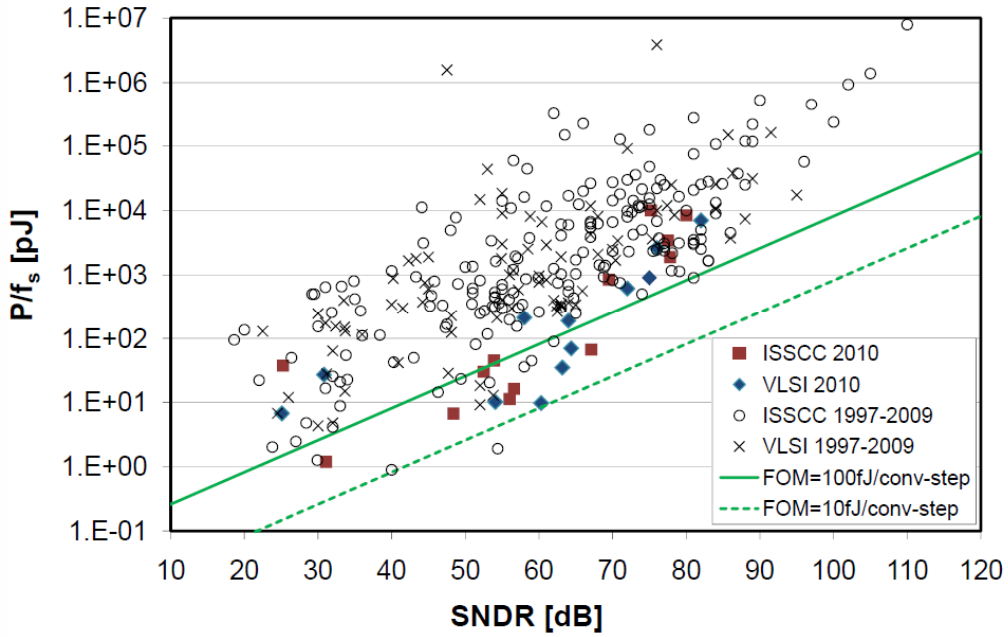


State-of-the-Art

- Performance of state-of-the-art ADCs ([1])



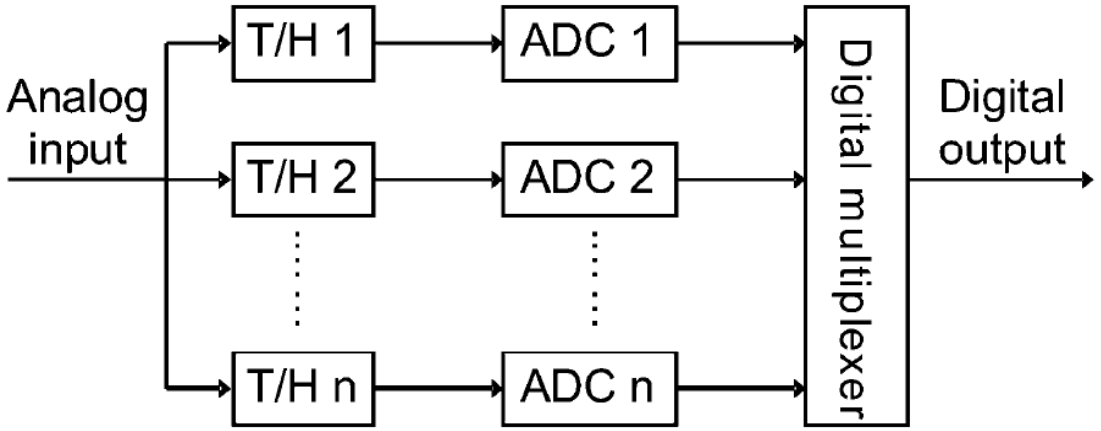
ISSCC 08~09



Ex.: [2] 1.8GS/s, 8bits, 420 mW
0.98 pJ/conversion step

Time-Interleaving Option

- Time-interleaving ADCs for achieving high SR and high SNDR

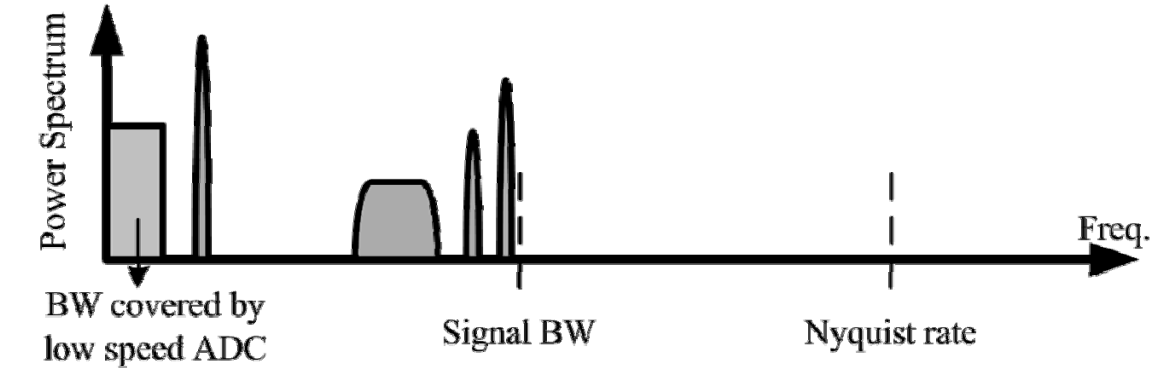


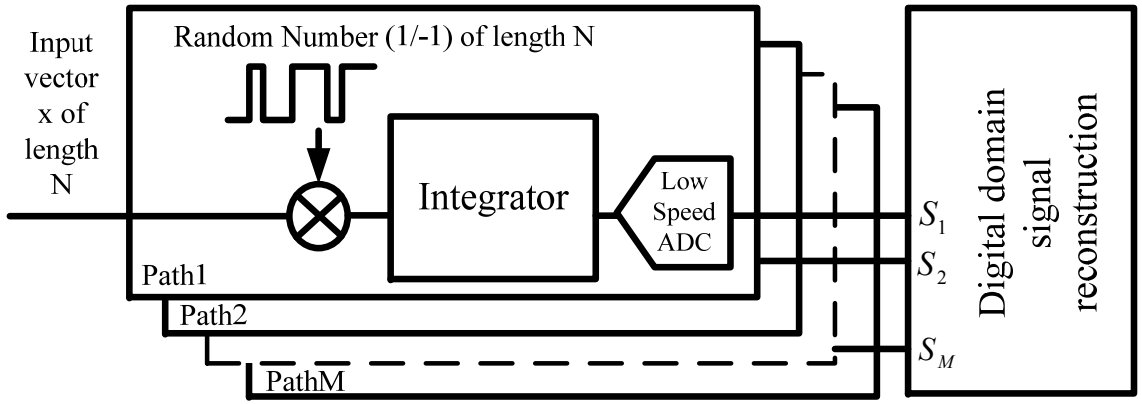
Time-interleaved ADC architecture.

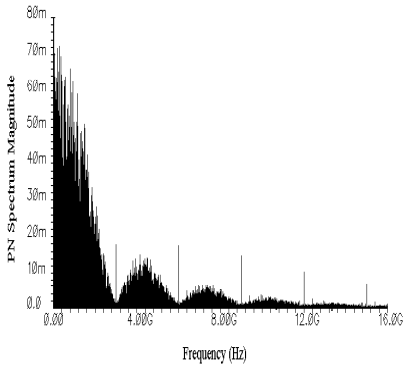
Ex.: [2] 1.8GS/s, 8bits, 420 mW
0.98 pJ/conversion step

Parallel CS Option

- Is that possible to sample the wideband sparse signal with low sampling rate?







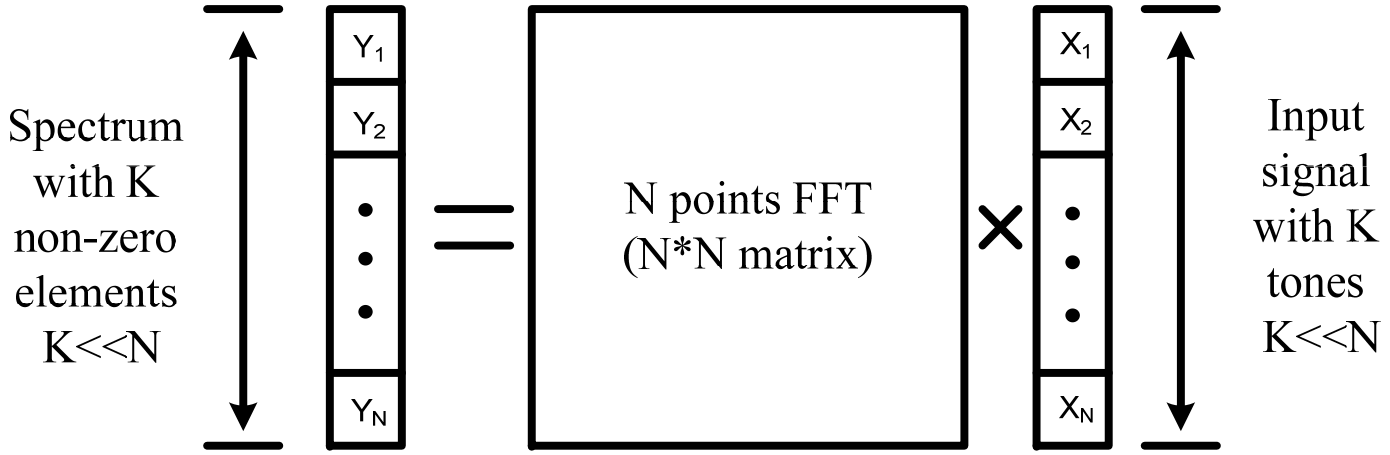
Power Spectral Estimation

Frequency domain sparse signal: $x \in R^{N\times 1}$

The N-points Fourier transform Matrix: $\psi \in C^{N\times N}$

The signal spectrum: $y = \psi x \quad y, \in R^{N\times 1}$

K non zero elements $K << N$



Matrix Notation

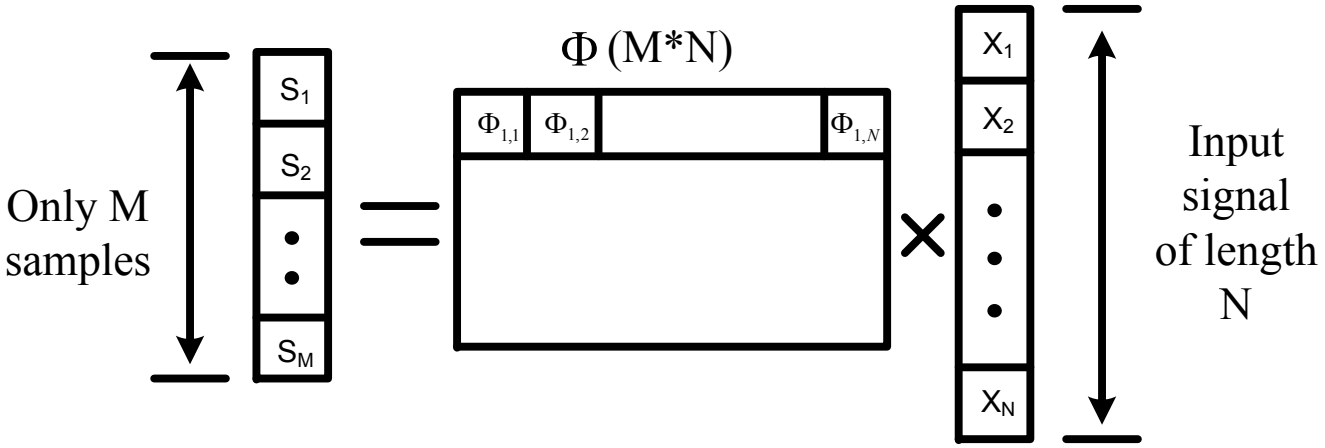
Frequency domain sparse signal: $x \in R^{N\times 1}$

The N-points Fourier transform Matrix: $\psi \in C^{N\times N}$

The signal spectrum: $y = \psi x \quad y, \in R^{N\times 1}$

K non zero elements, *K* << *N*

Vector to be sampled: $s = \Phi x \quad s \in R^{M\times 1} \quad \Phi, \in R^{M\times N}$ *M* << *N*



Signal Reconstruction

Frequency domain sparse signal: $x \in R^{N\times 1}$

The N-points Fourier transform Matrix: $\psi \in C^{N\times N}$

The signal spectrum: $y = \psi x \quad y \in R^{N\times 1}$

K non zero elements, *K* << *N*

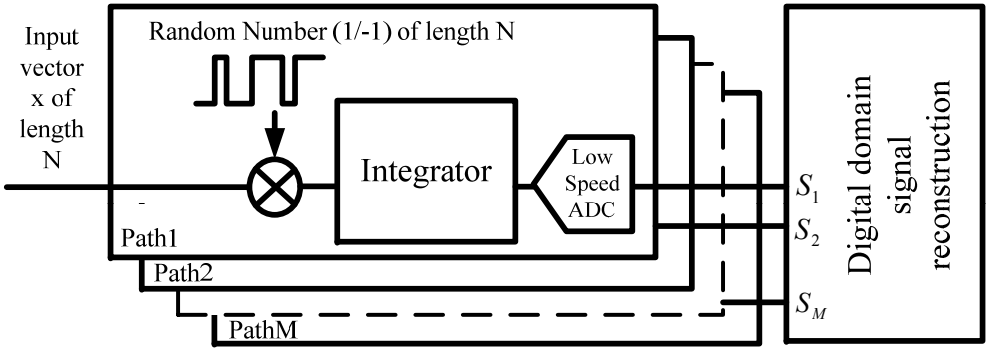
Vector to be sampled: $s = \Phi x \quad s \in R^{M\times 1} \quad \Phi \in R^{M\times N}$ *M* << *N*

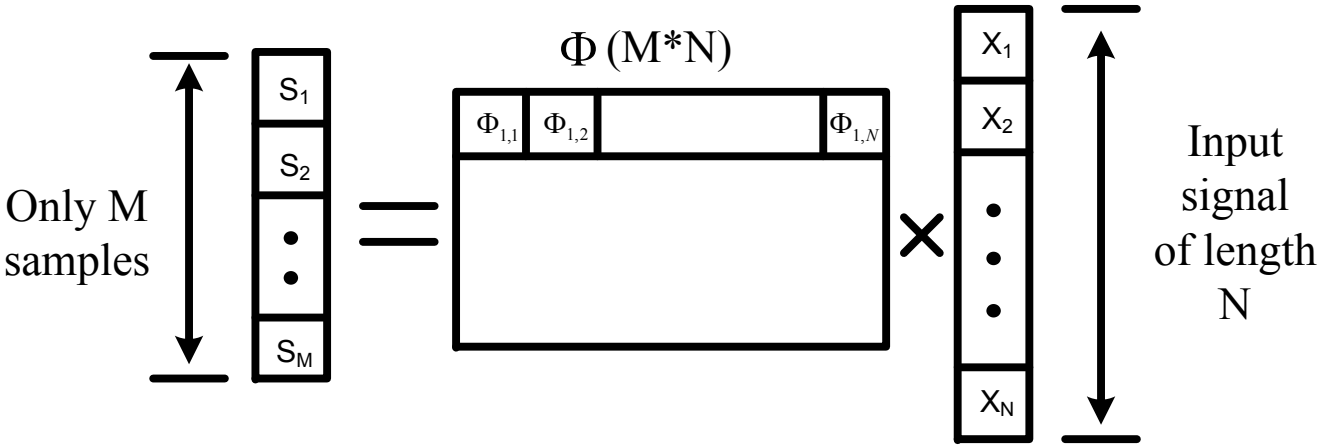
$$\Phi \psi^H y = s$$

$$y = \arg\ \min \|y\|_1 \quad s.t.\ \ \Phi \psi^H y = s \qquad M \geq K \log_2 (N/K)$$

System Level Implementation

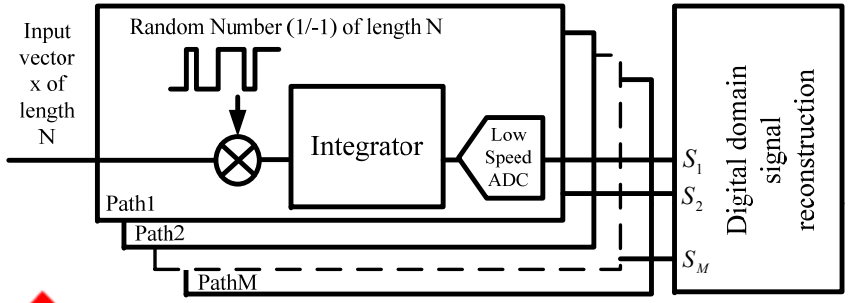
- System level architecture of a CS data acquisition system



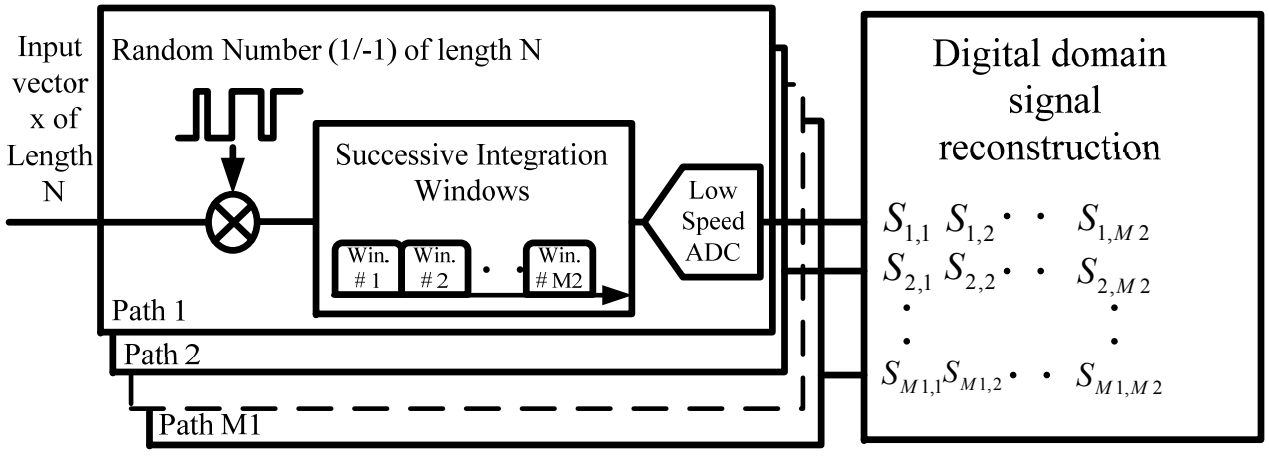


Analog Windowing

- Segmented integration windows for reducing # of paths (PSCS)[5]



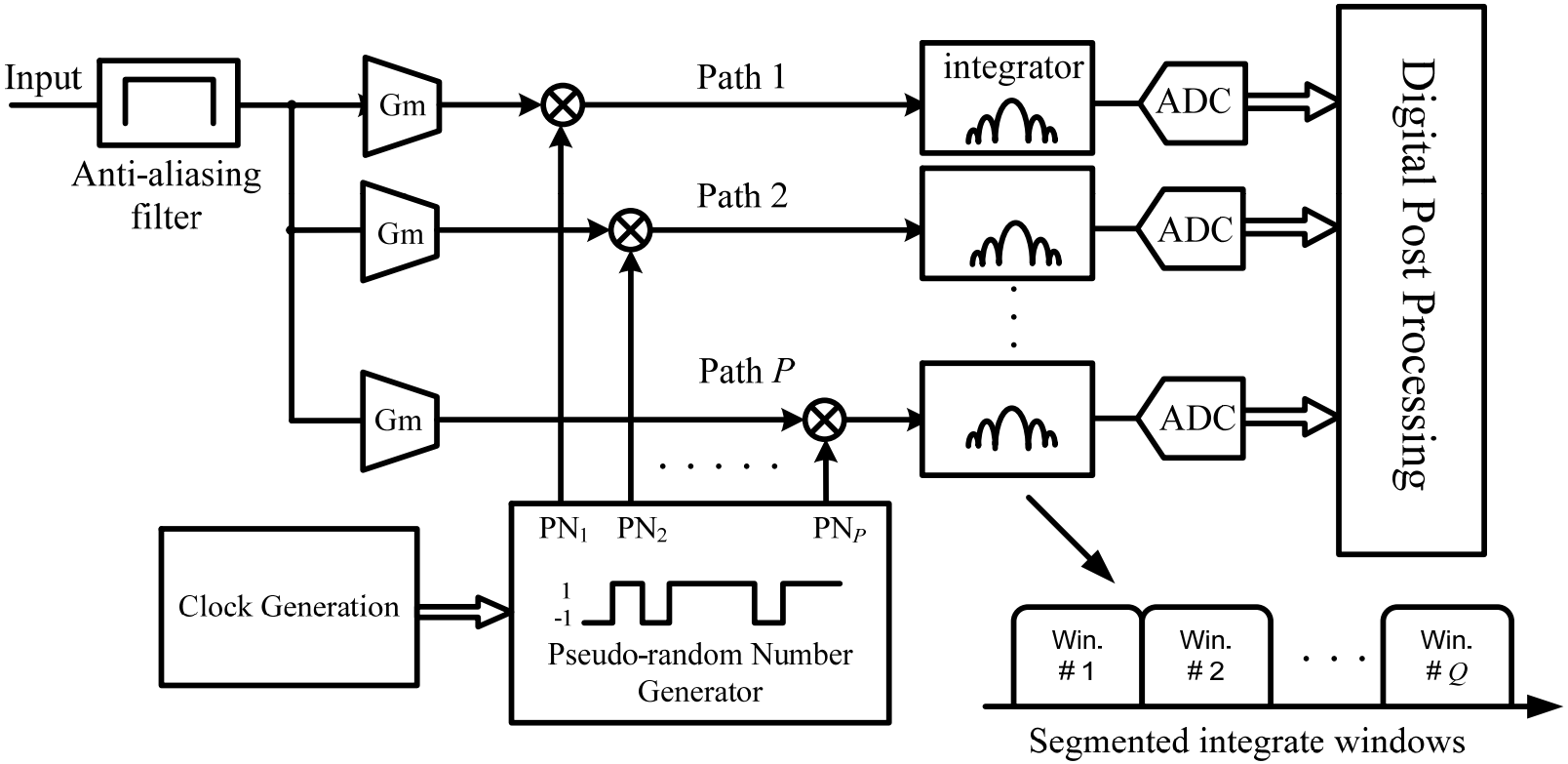
$$M \geq K \log_2 (N/K)$$



M1*M2=M

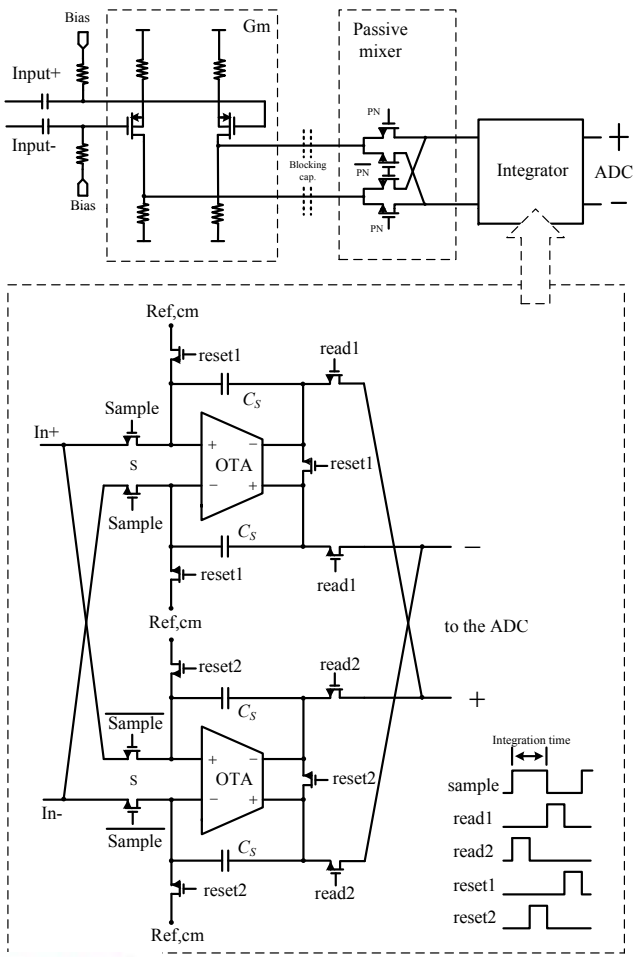
System Level Diagram

- System level diagram

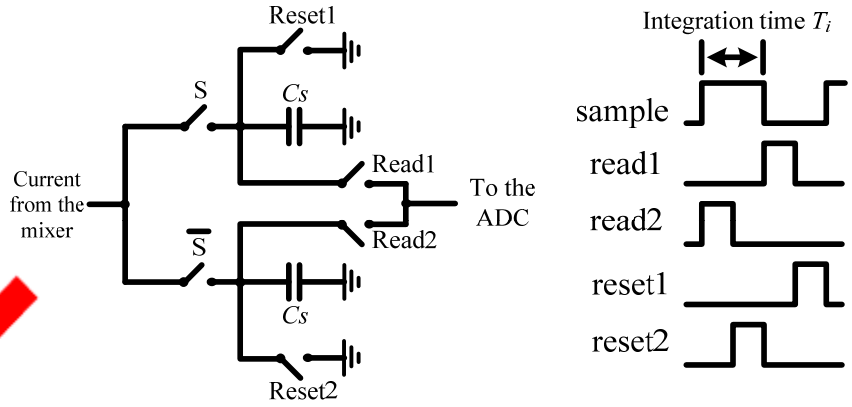


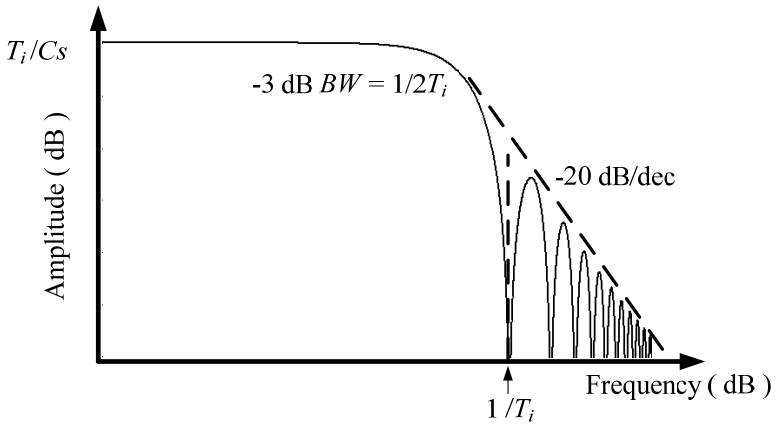
Circuit Level Implementation

- One path circuit



Simplified integrator schematic

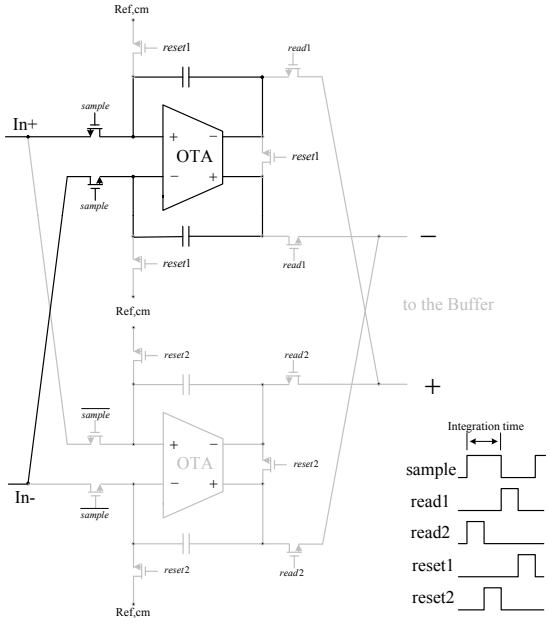




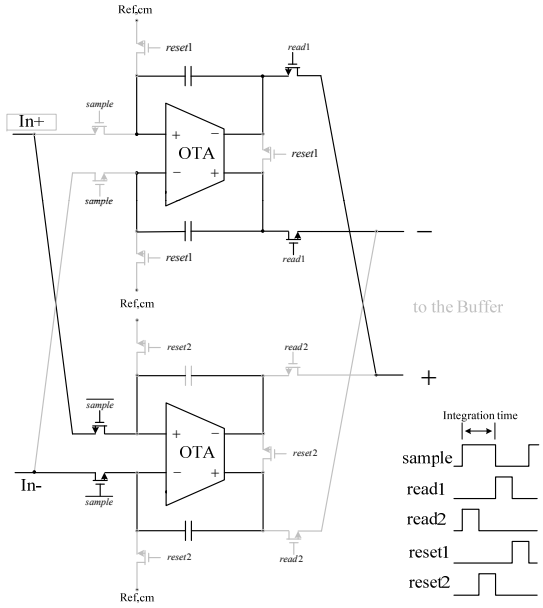
Frequency response of the integrator

Circuit Level Implementation

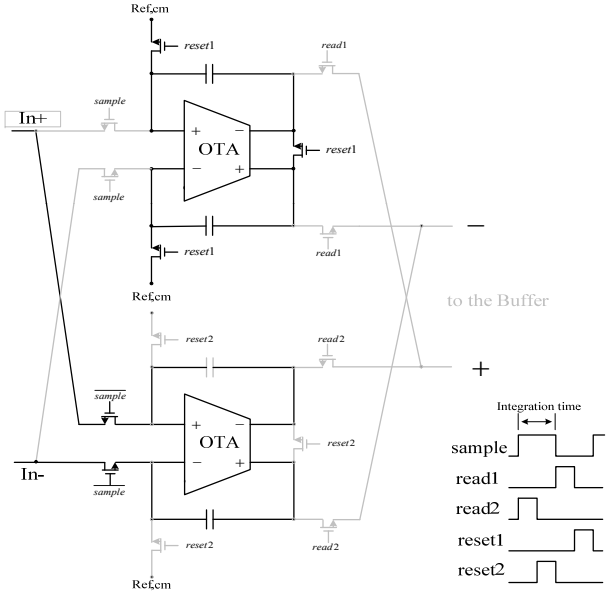
- Operation of the differential active integrator



Integrating in the upper branch



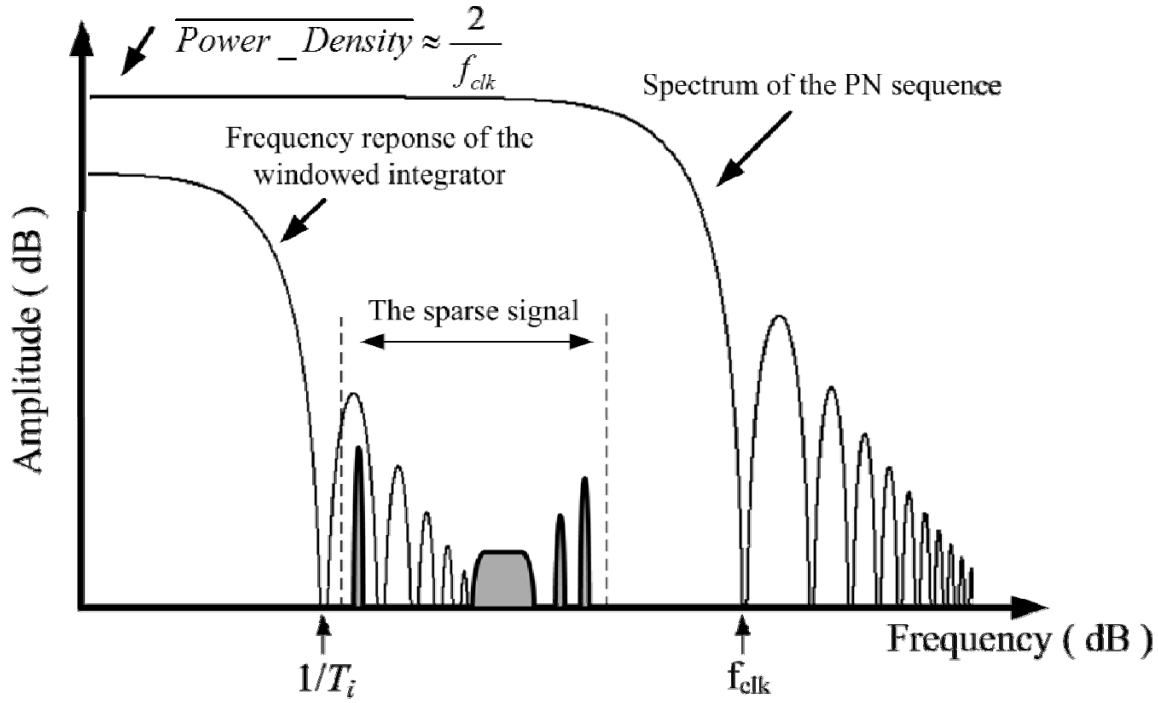
Read out integrated data In the upper branch and start to integrate in the lower branch



Reset the upper branch

Analysis

- The Signal gain of the front-end

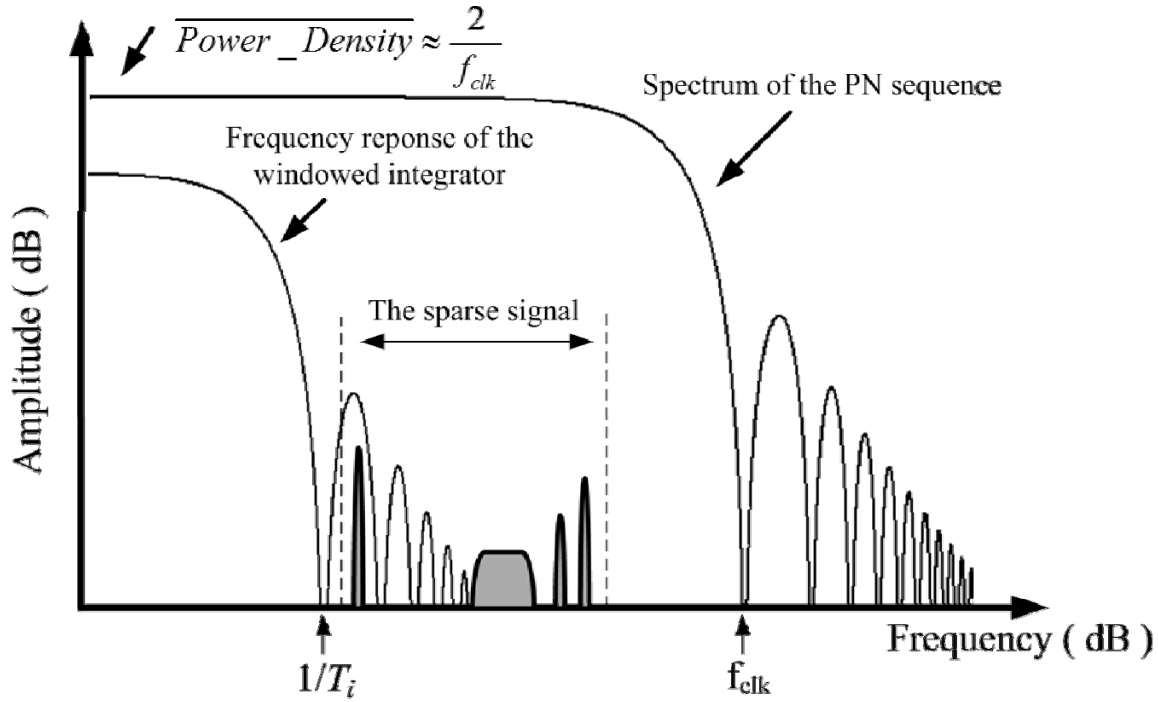


$$\left|Gain_S\right|^2 = \frac{V_{sig,output}^{\ 2}}{V_{sig,input}^{\ 2}}.$$

$$\left|Gain_S\right|^2 = \frac{\int_0^{\infty} \left[V_{sig,input}^{\ 2}(f)\,Gm^2\right] * \overline{PN^2(f)}\left|H_i(f)\right|^2 df}{\int_{10MHz}^{1.5GHz} V_{sig,input}^{\ 2}(f)\,df}.$$

Analysis

- Signal gain of the front-end



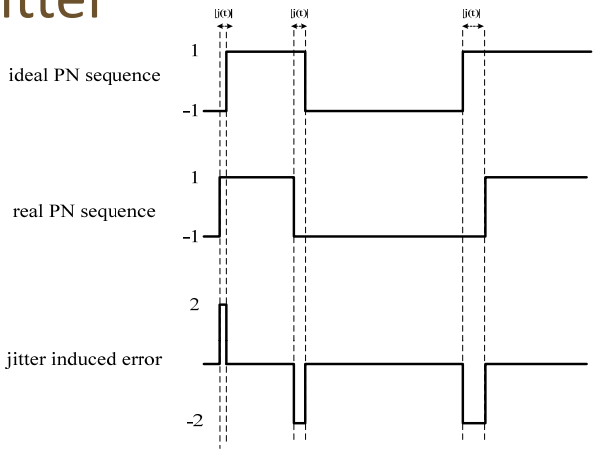
$$\left|Gain_S\right|^2 = \frac{V_{sig,output}^{\ 2}}{V_{sig,input}^{\ 2}}.$$

$$\left|Gain_S\right|^2 = \lambda\left(\frac{1}{C_s}\right)^2 T_i \frac{\left|Gm\right|^2}{f_{clk}}$$

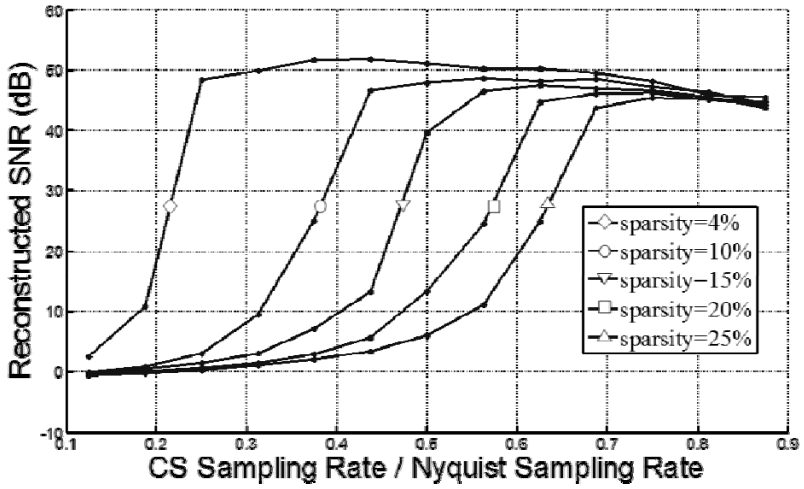
0.4< λ<1, λ=0.67 with normally distributed input

Jitter and SNR

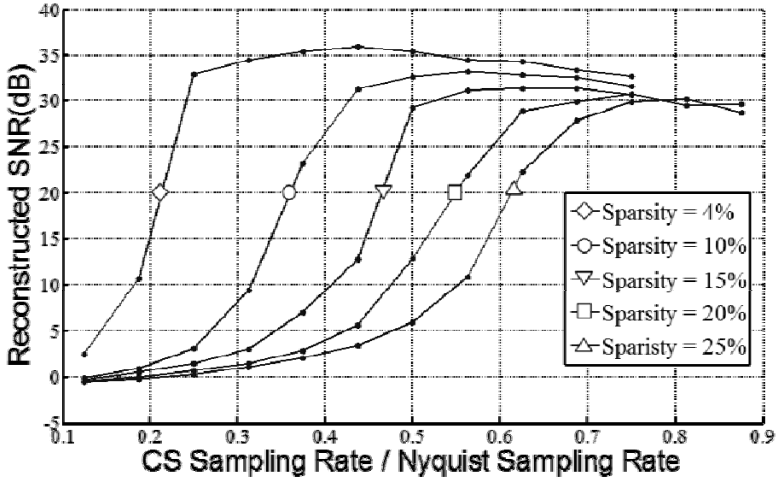
- Jitter



$$\mathrm{SNR_j} = \frac{V_{sig,output}^{\ 2}}{N_j^{\ 2}} = \frac{\lambda}{2\sigma_j^2 f_{clk}^{\ 2}}.$$



The reconstructed SNR with 0.5 ps jitter, 3G PN

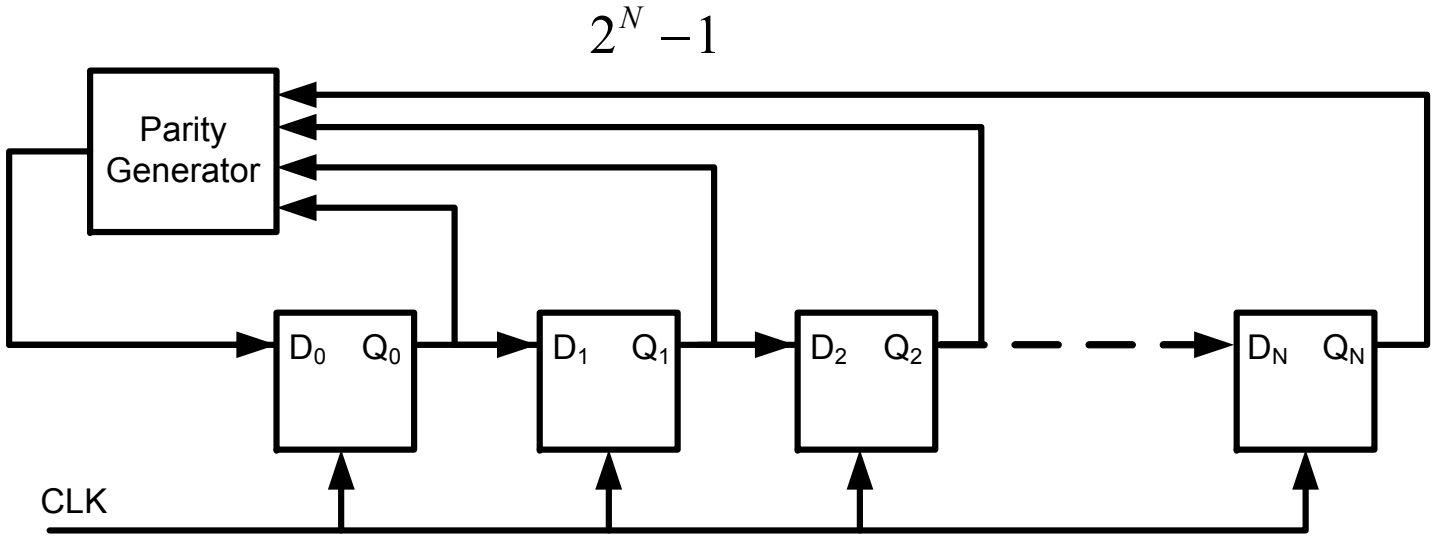


The reconstructed SNR with 3 ps jitter 3G PN

PN Generator: The Speed and Power Bottleneck

- The PN generator

Limiting the signal bandwidth and reconstructed signal quality



3G~4G with 90nm CMOS

Signal Reconstruction

- Introduction

$$\Phi \psi^H y = s$$

$$y = \arg \min \|y\|_1 \quad s.t. \quad \Phi \psi^H y = s$$

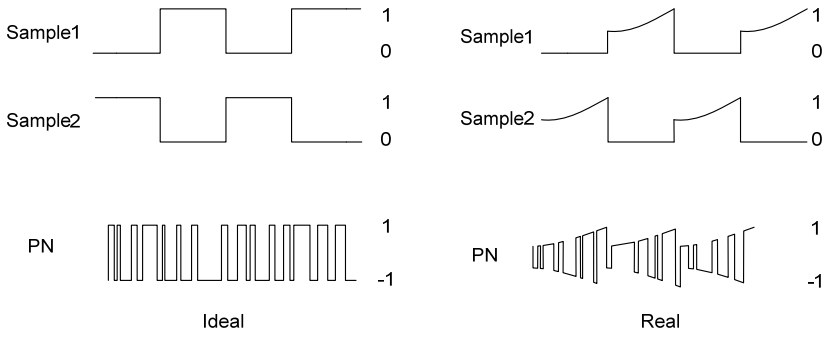
PN Sequence Imperfections

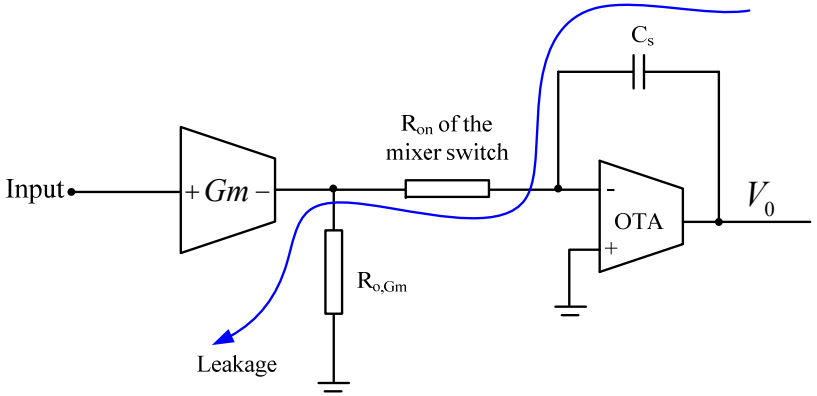
- Introduction

$$\Phi \psi^H y = s$$

$$y = \arg \min \|y\|_1 \quad s.t. \quad \Phi \psi^H y = s$$

- In reality, the PN sequence that is applied to the circuit is distorted (ex. charge leakage)





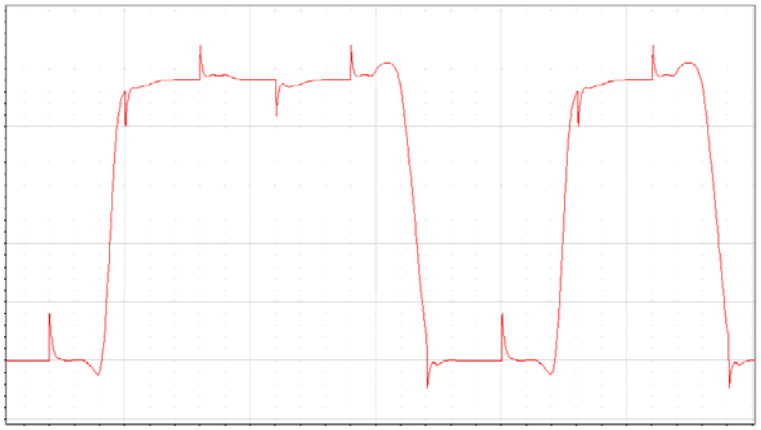
PN Sequence Imperfections

- Introduction

$$\Phi \psi^H y = s$$

$$y = \arg \min \|y\|_1 \quad s.t. \quad \Phi \psi^H y = s$$

- In reality, the PN sequence that is applied to the circuit is distorted (ex. Finite rising/falling time)

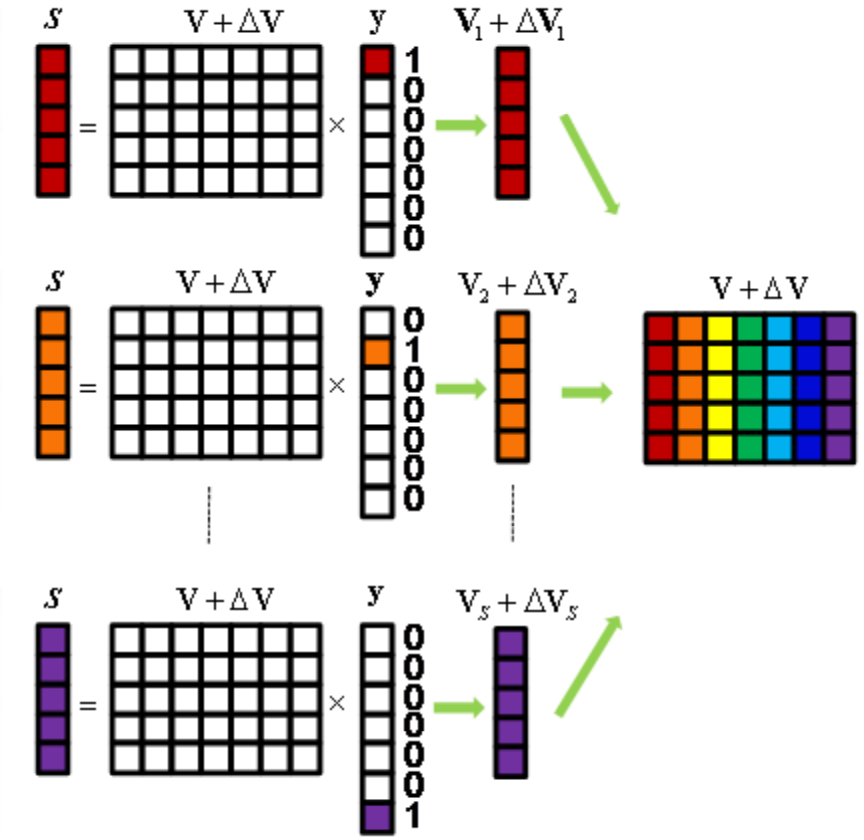


Signal Reconstruction

- Direct Training

$$\Phi \psi^H y = s$$

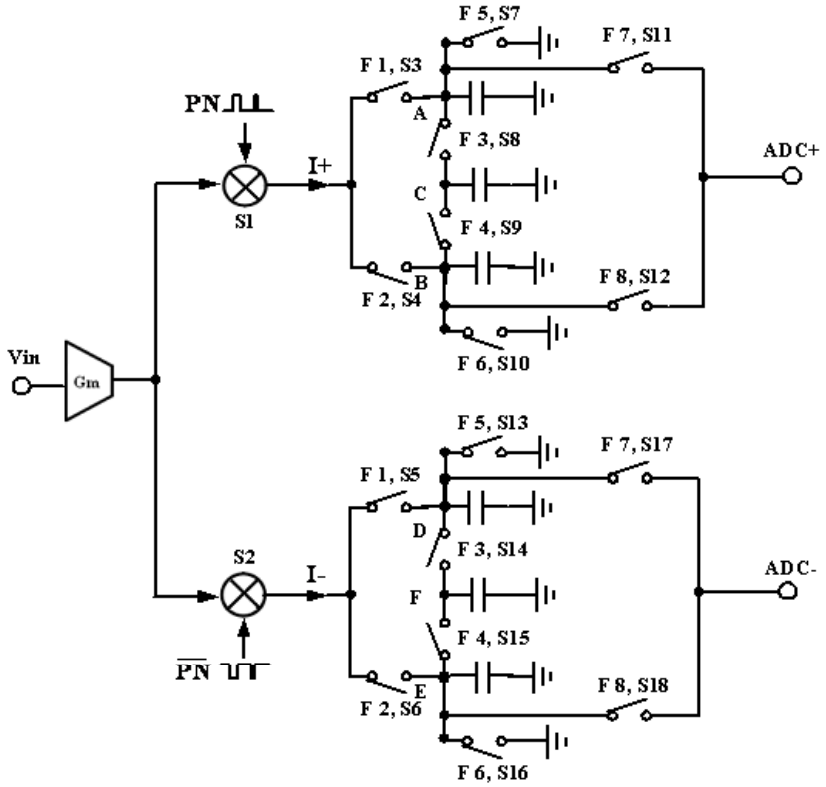
V+DV: $\Phi \psi^H$

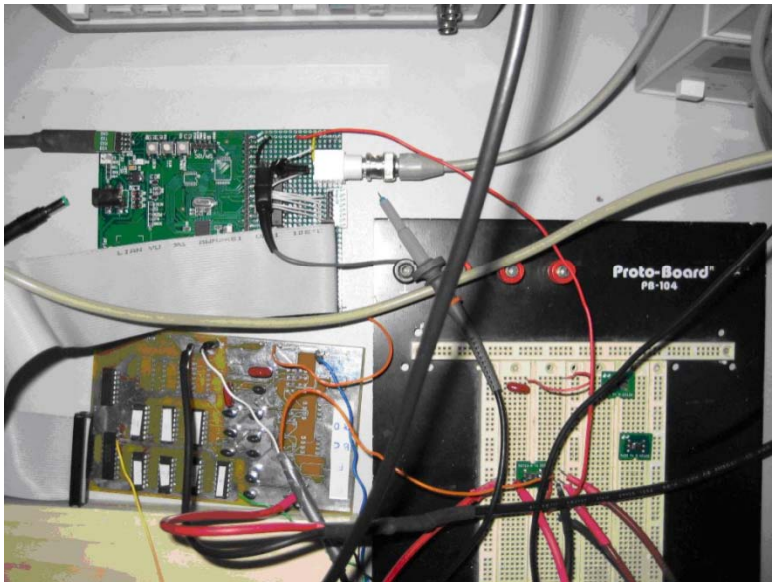


A CS Front-end with Discrete Components

- A low frequency BPSK communication system

S	K	Δf	BW	T=1/Δf	N	Δt=T/M	fs=1/Δt	OVR	BER
100	5	2KHz	200KHz	500μs	4	31.25 μs	32KHz	15.34%	5.36E-4

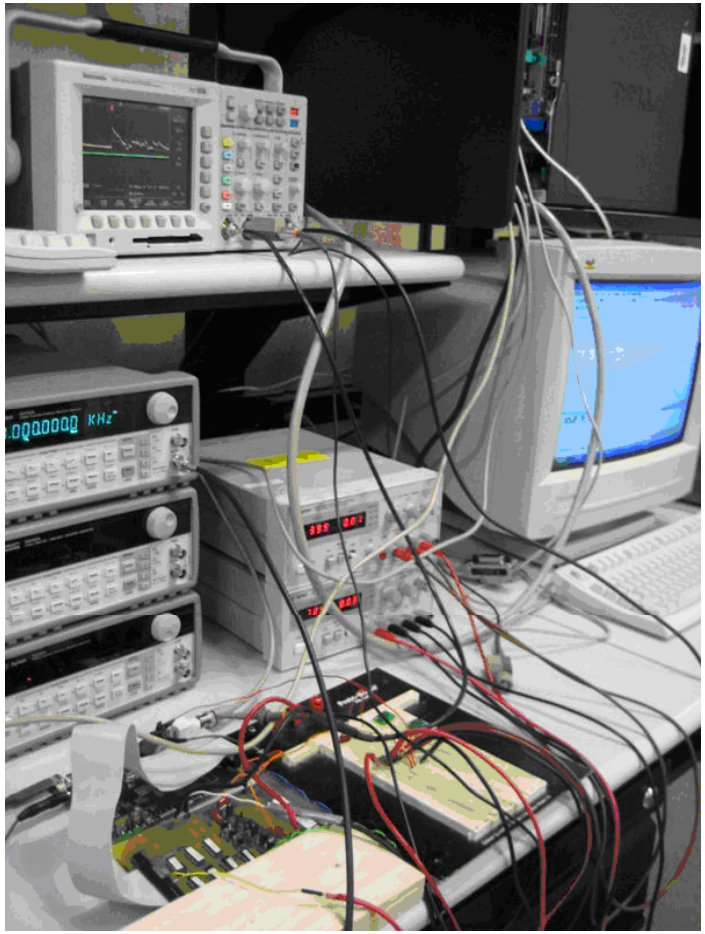


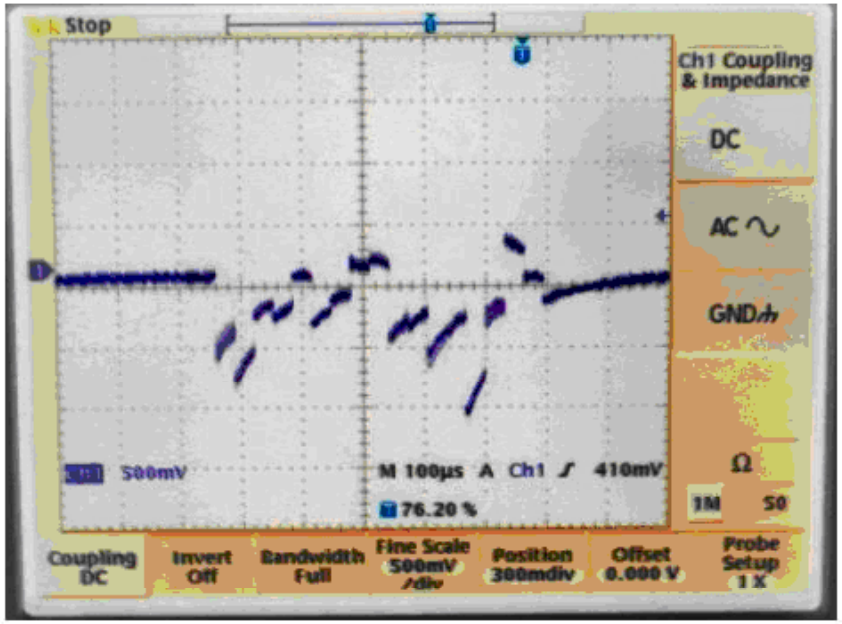


Gm: TIOPA861, 116 mS
Switches: CD4066BCN
Sampling Capacitor: 17 nF

A CS Front-end with Discrete Components

- A low frequency BPSK communication system





An example of the output waveforms

A GHz CS Front-end with 90nm CMOS

- System level parameters, with IBM 90nm CMOS process

Input Signal Bandwidth	10 MHz ~ 1.5 GHz
Number of Parallel Paths	8
Single Path sampling rate (10/256 signal sparsity)	110 Ms/s
Overall System Sampling rate	880 MS/s (29% Nyquist Rate)
SNDR with 0.5 ps jitter	44 dB
Max. signal gain at the front-end	around 20 dB
Fullscale input / output	-20 dBm / -2 dBm (referred to 50 ohms) 0.06 / 0.5Vpp

A GHz CS Front-end with 90nm CMOS

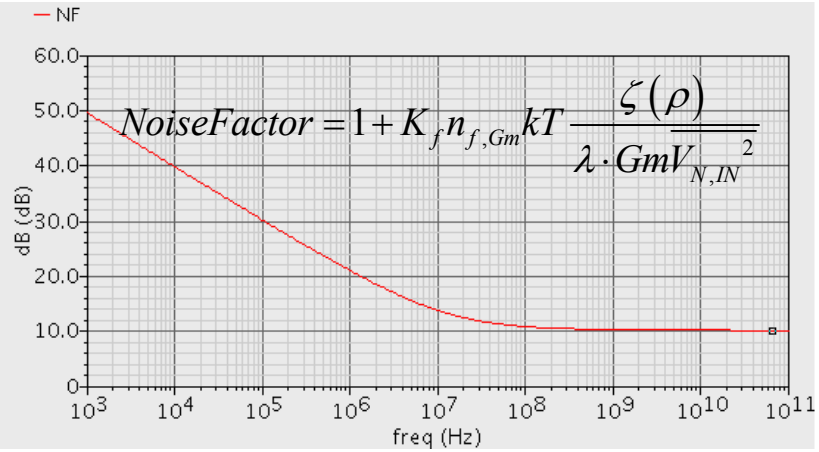
- Circuit block parameters

Gm	6.5 mS
NF of Gm / IIP3	11.1 dB / 6 dBm
DC Gain of the OTA	37 dB
GBW of the OTA	250M
SNDR of the OTA	> 50 dB
Phase margin of the OTA	69 degree
Sampling capacitor	1 pF

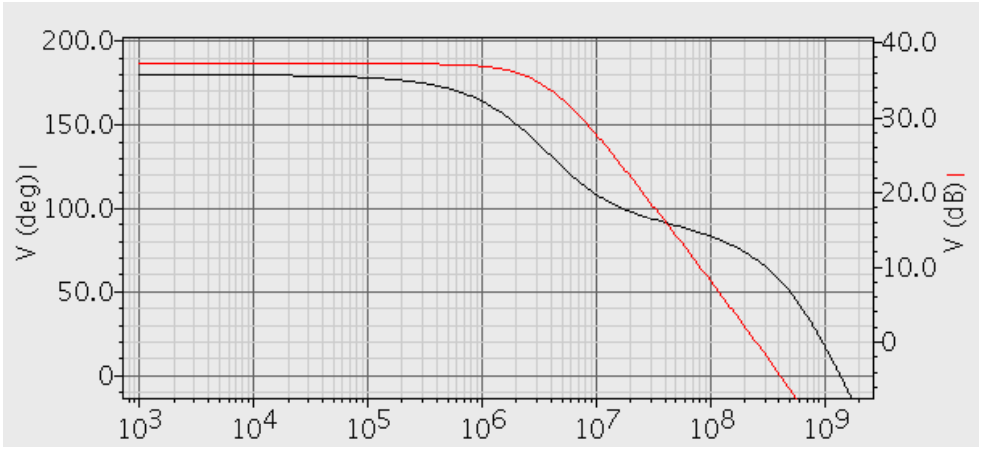
Those numbers are determined by equations in Part III

Simulations

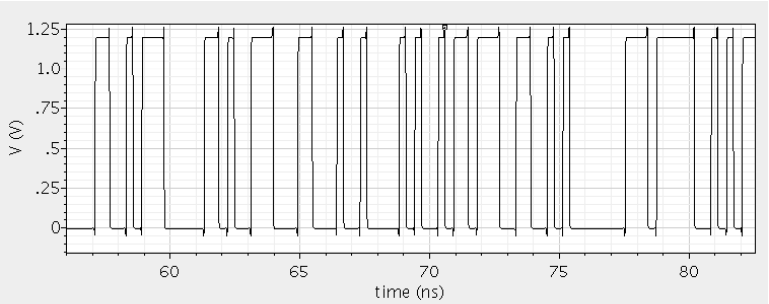
- Block Level Simulations



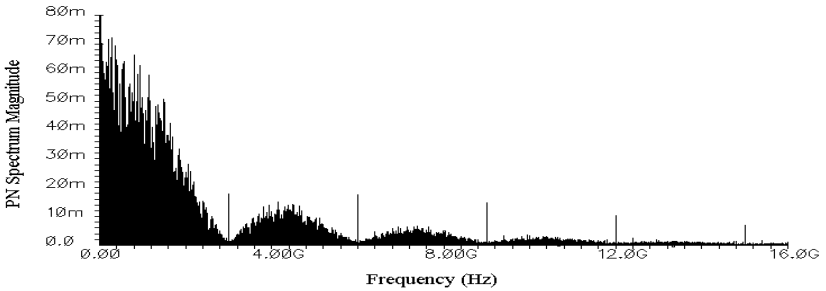
NF of the Gm stage



Bode plot of the OTA



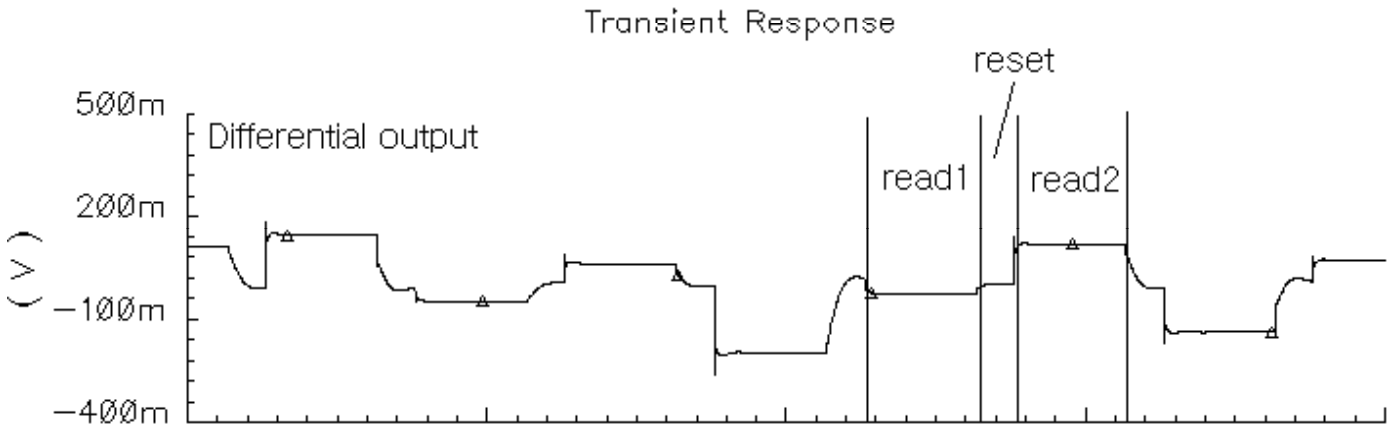
3 GS/s PN sequence



Spectrum of the generated PN

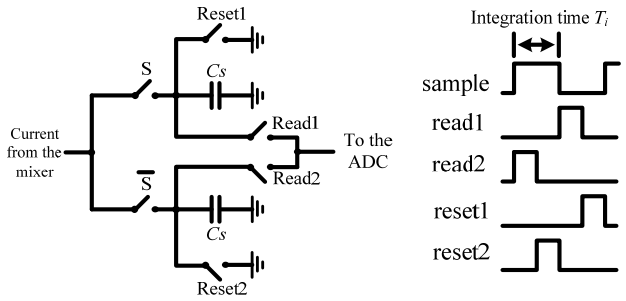
Simulations

- Block Level Simulations



An example of the output waveform obtained in simulation

Reconstructed SNR = 40 dB with sampled data from coarse transient simulation



Comparison with State of the Art

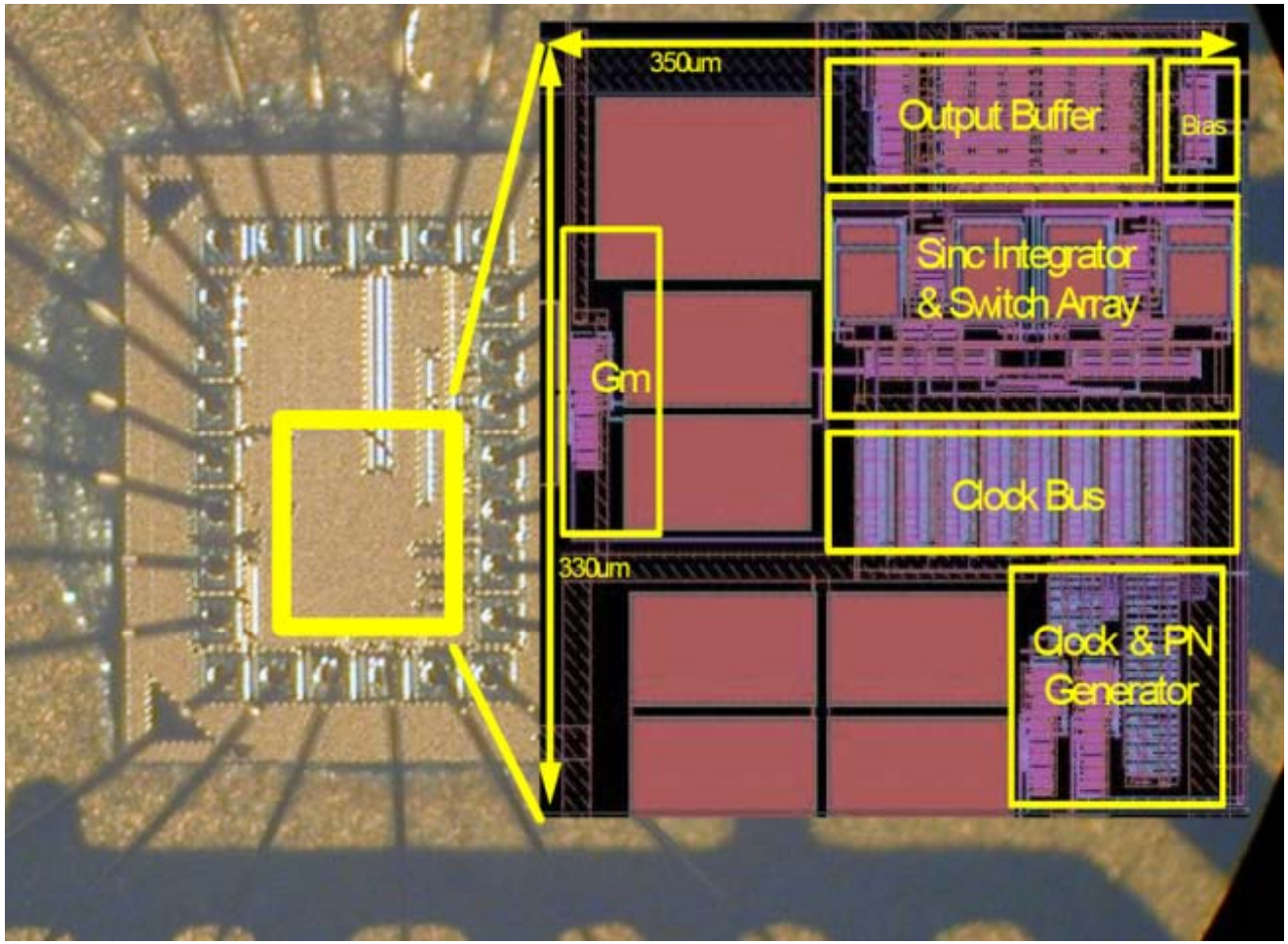
- Power consumption & comparison with other works

Power consumption	Gm stages	16 mW
	Integrators	19.2 mW
	Clocks	57.6 mW
	PN sequences	
	ADCs	28 mW
	Overall	120.8 mW

Design	[7]	[6]	[2]a	[2]b	[8]	This work
Sampling Rate (GS/s)	1	0.8	1.35	1.8	3.5	3
ENOB (SNDR in dB)	8.8 (55)	9 (56)	7.7 (48.2)	7.9 (49.4)	4.9 (31.18)	7 (44)
Power consumption (mW)	250	350	180	420	98	120.8
Process(nm)	130	90	130	130	90	90
FOM （pJ/conversion step）	0.56	0.85	0.64	0.98	0.94	0.31
Signal Sparsity	Arbitrary					4%
, where P is the power and SR is the ADC sampling rate.						

$$FOM = \frac{P}{2^{ENOB} SR}$$

Die Photo

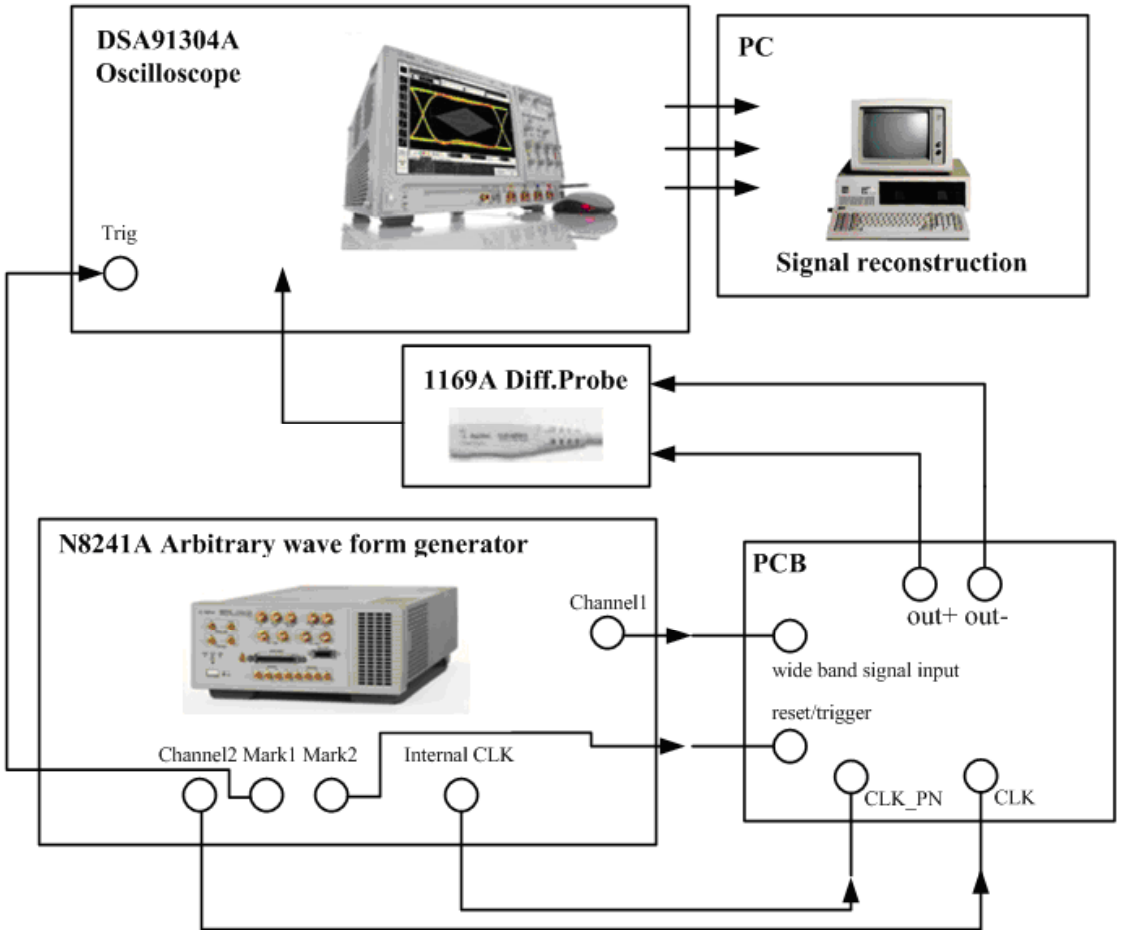

350um
Output Buffer
Bias
Sinc Integrator
& Switch Array
Gm
Clock Bus
330um
Clock & PN
Generator

Testing

- Test bench diagram

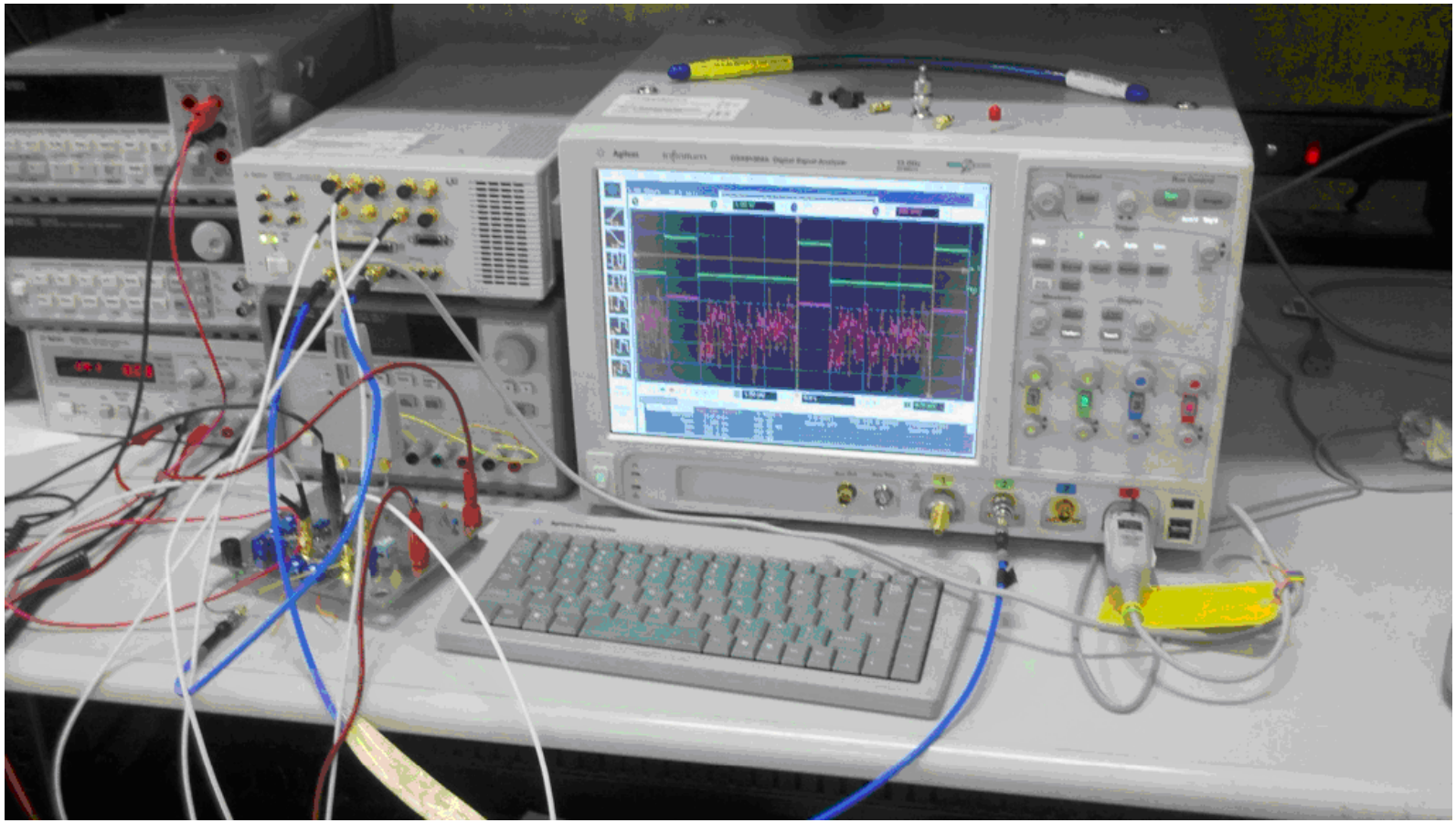
PN jitter 4.13 ps
Max PN speed 1.25G
Max signal BW 500M

Target: 41 dB SNR
1GS/s equivalent
Sampling rate



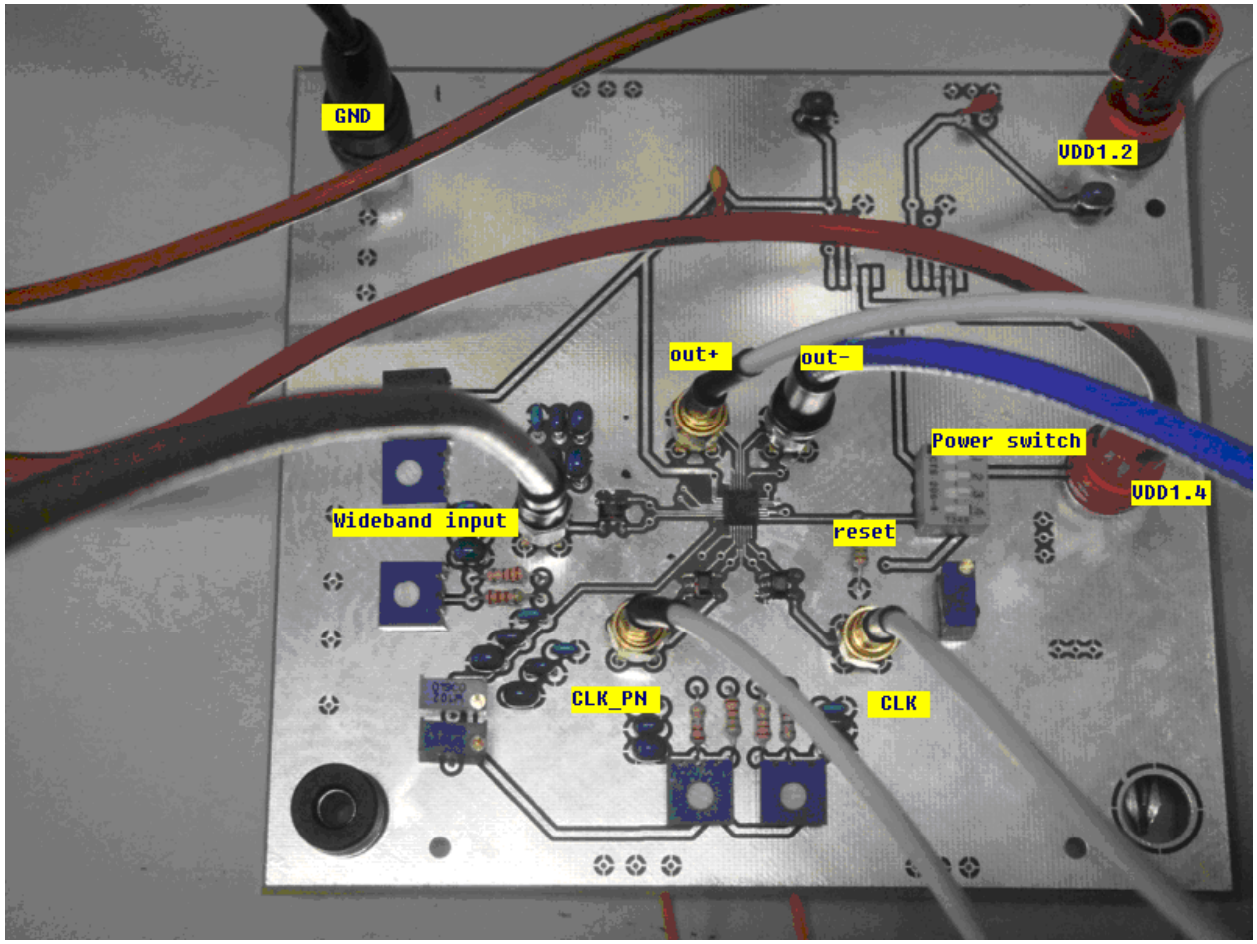
Testing

- Test bench



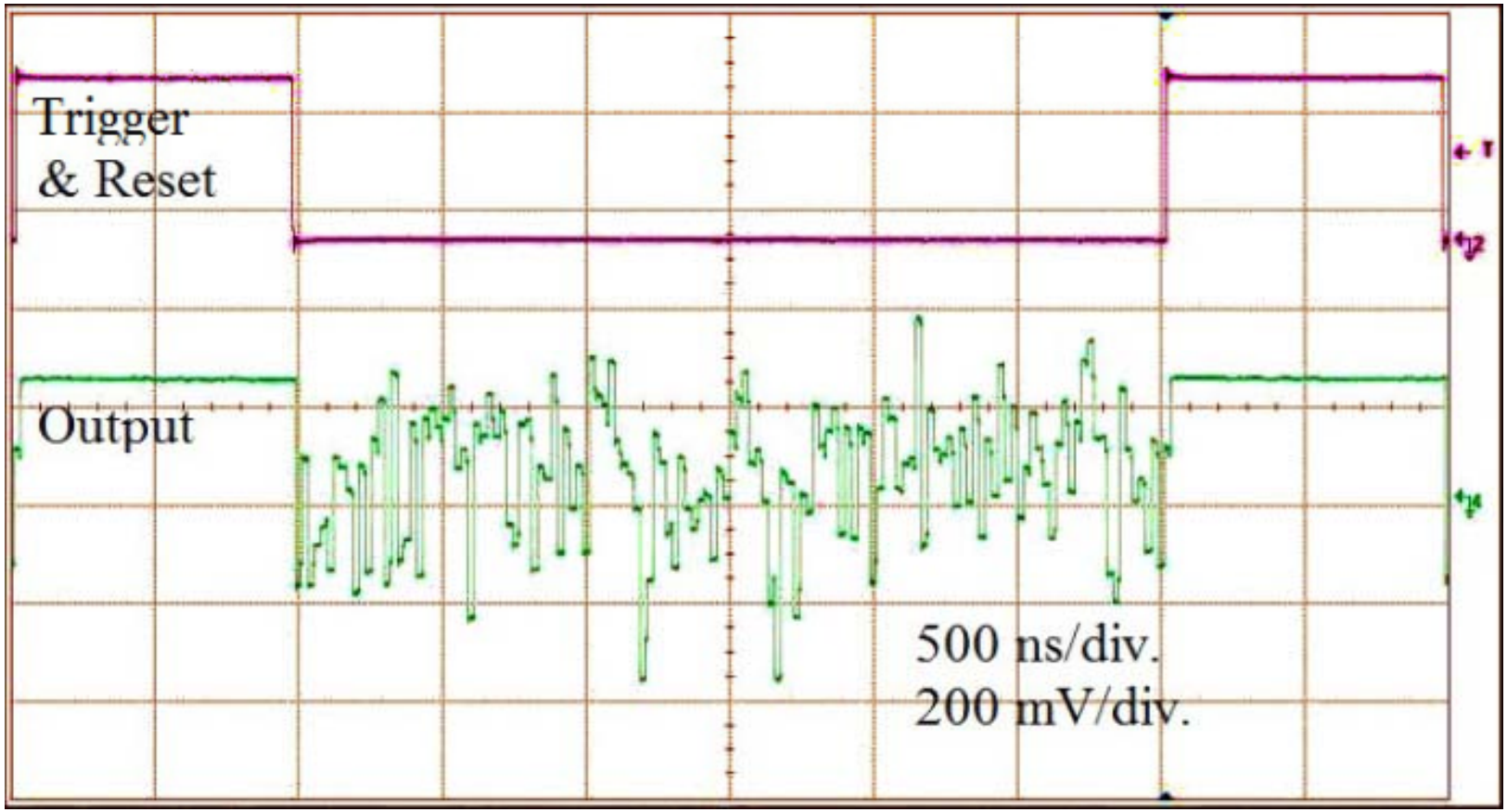
Board

- PCB


GND
VDD1.2
out+
out-
Power switch
VDD1.4
Wideband input
reset
CLK_PN
CLK

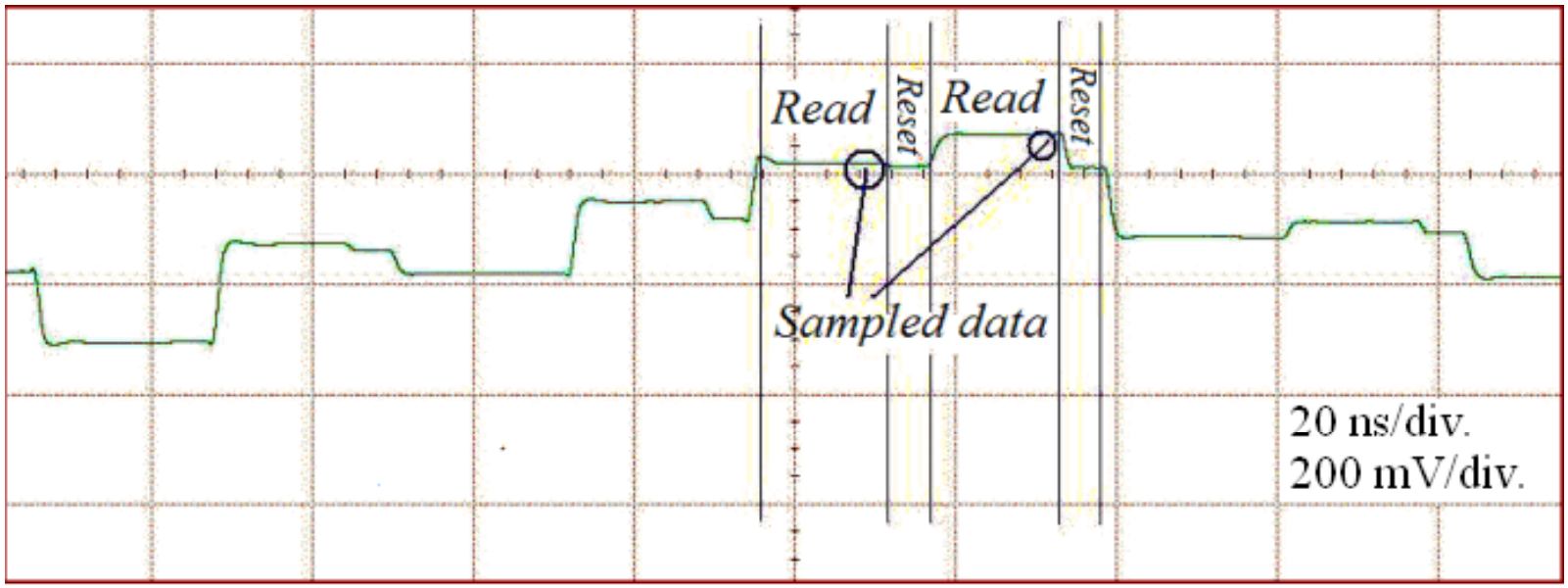
Waveforms

- The output waveform



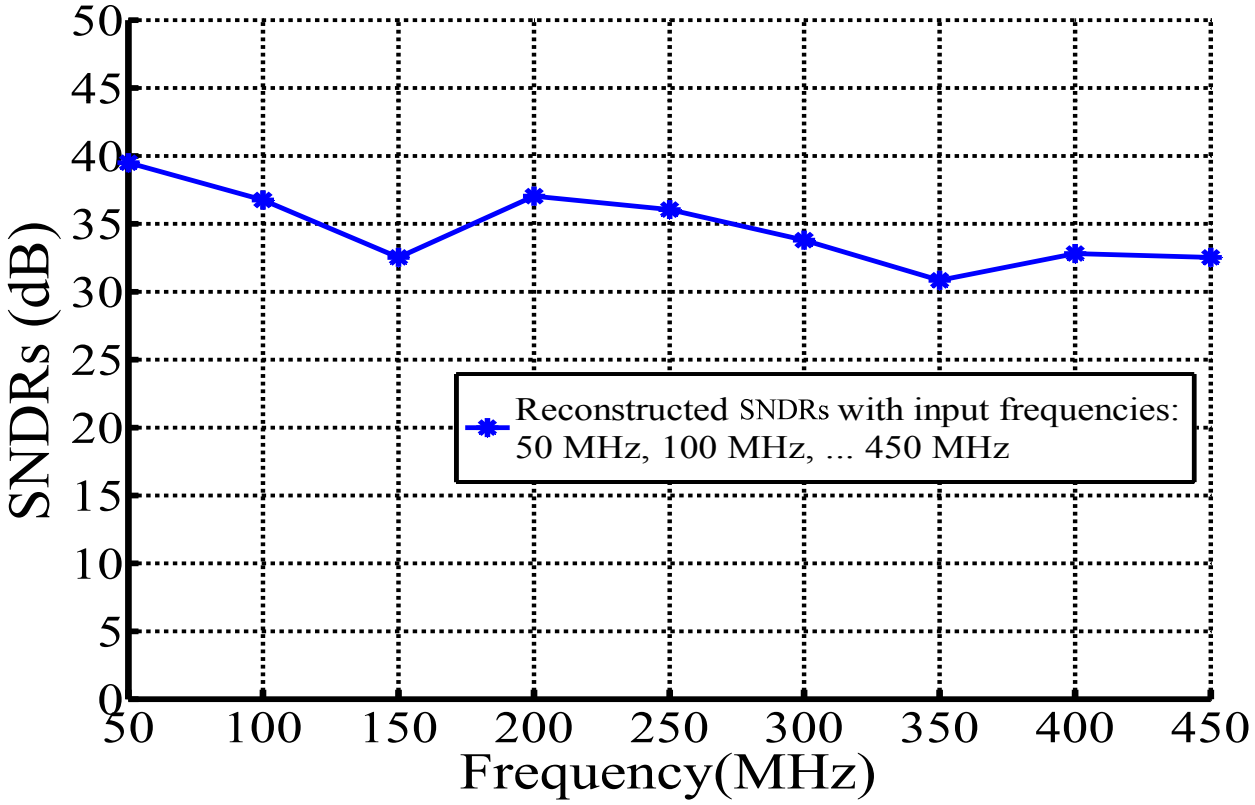
Waveforms

- The output waveform



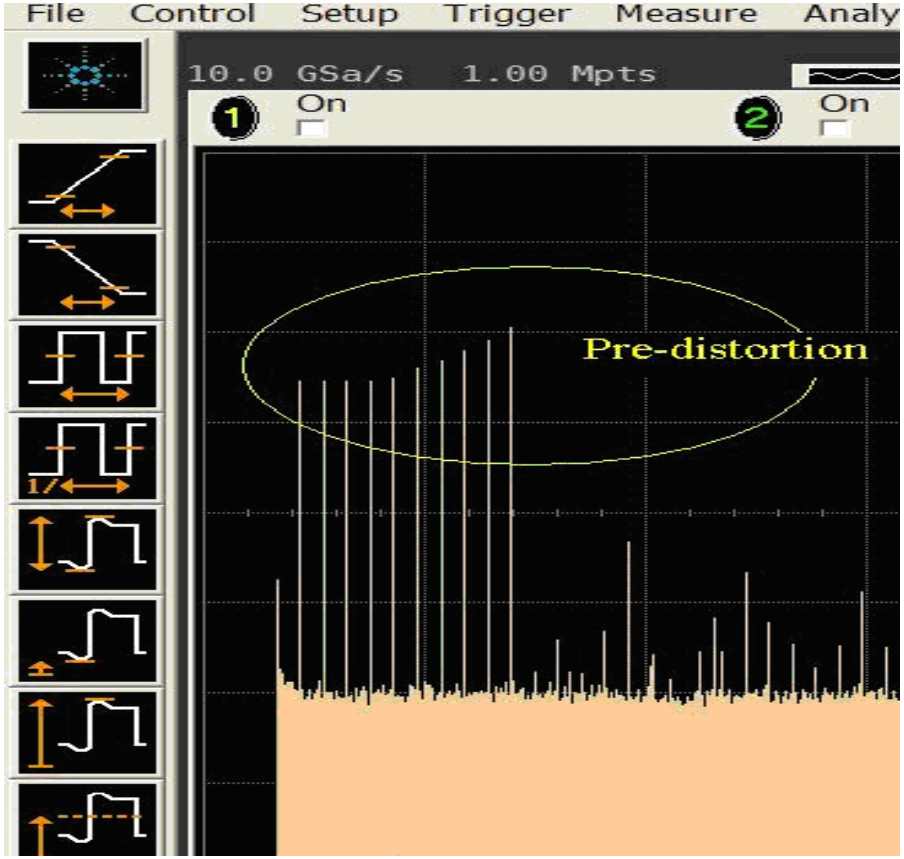
Performance

- Reconstructed SNR vs. frequency (single tone test)



Predistortion for Calibration

- Reconstructed Spectrums (Multi-tone test)



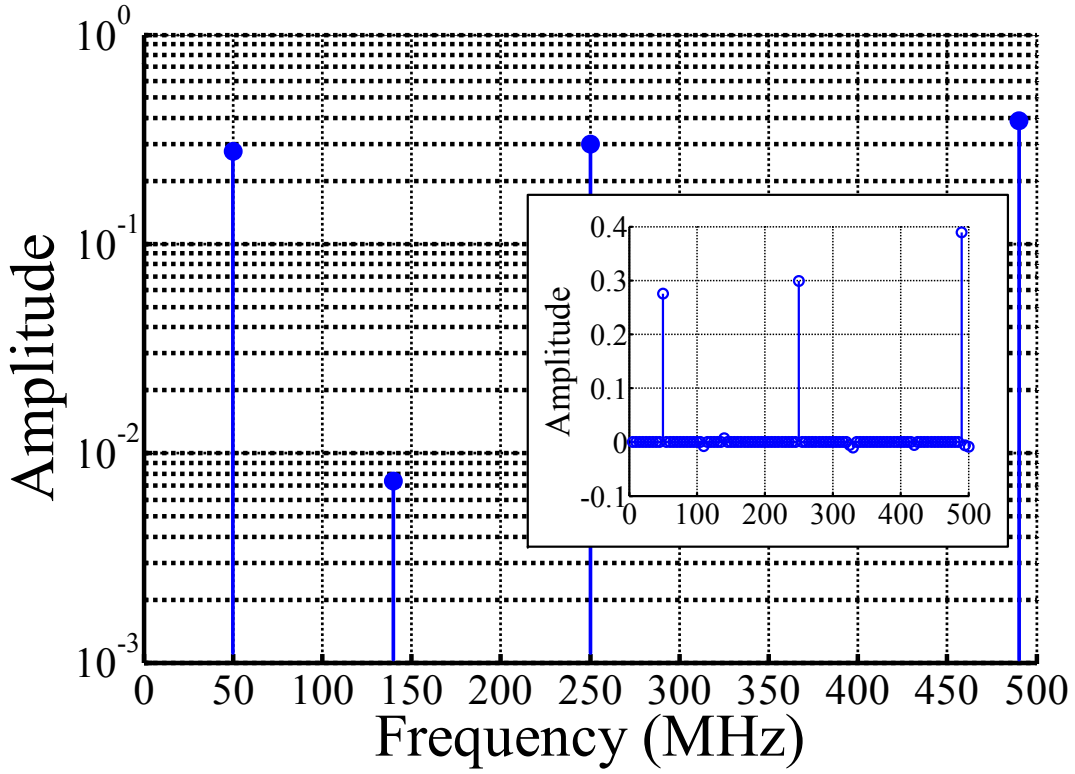
Differential amplitudes are introduced by pre-distortion of the AWG

Performance

- Reconstructed Spectrums (Multi-tone test)

Case 1: 50, 250, 490

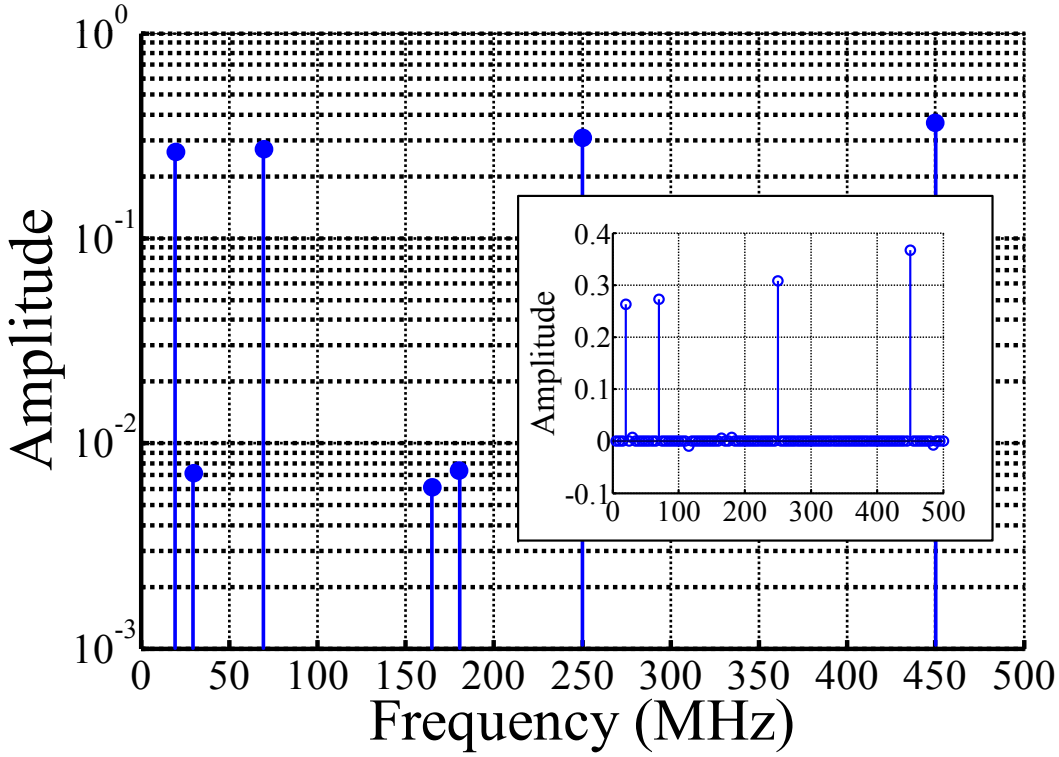
The reconstructed SNR= 29.26dB



Performance

- Reconstructed Spectrums (Multi-tone test)

Case 2: 20, 70, 250, 450
The reconstructed SNR=27.74dB

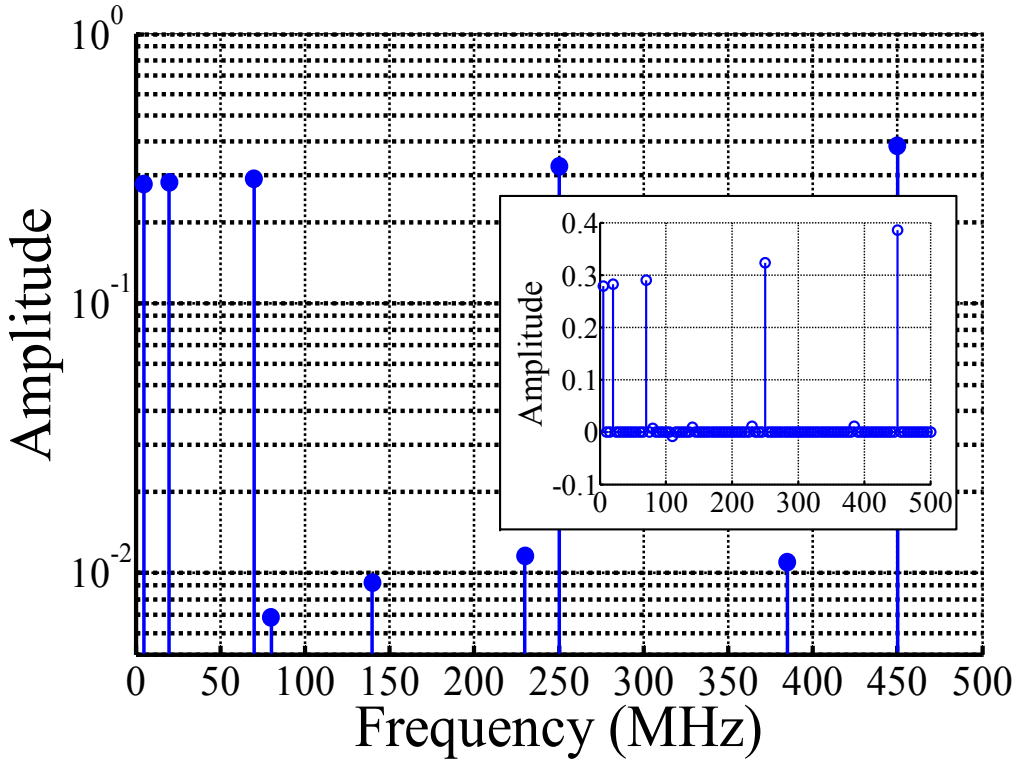


Performance

- Reconstructed Spectrums (Multi-tone test)

Case 3: -20, -70, 250, 450

The reconstructed SNR= 24.53 dB



Comparison with State of the Art

- Comparison table

Design	[7]	[6]	[2]a	[2]b	[8]	This work (sim)	This work (tested)
Sampling Rate (GS/s)	1	0.8	1.35	1.8	3.5	3	1
ENOB (SNDR in dB)	8.8 (55)	9 (56)	7.7 (48.2)	7.9 (49.4)	4.9 (31.18)	7 (44)	6 (38)
Power consumption (mW)	250	350	180	420	98	120.8	60
Process(nm)	130	90	130	130	90	90	90
FOM （pJ/conversion step）	0.56	0.85	0.64	0.98	0.94	0.31	0.9
Signal Sparsity	Arbitrary					4%	4%

where P is the power and SR is the ADC sampling rate.

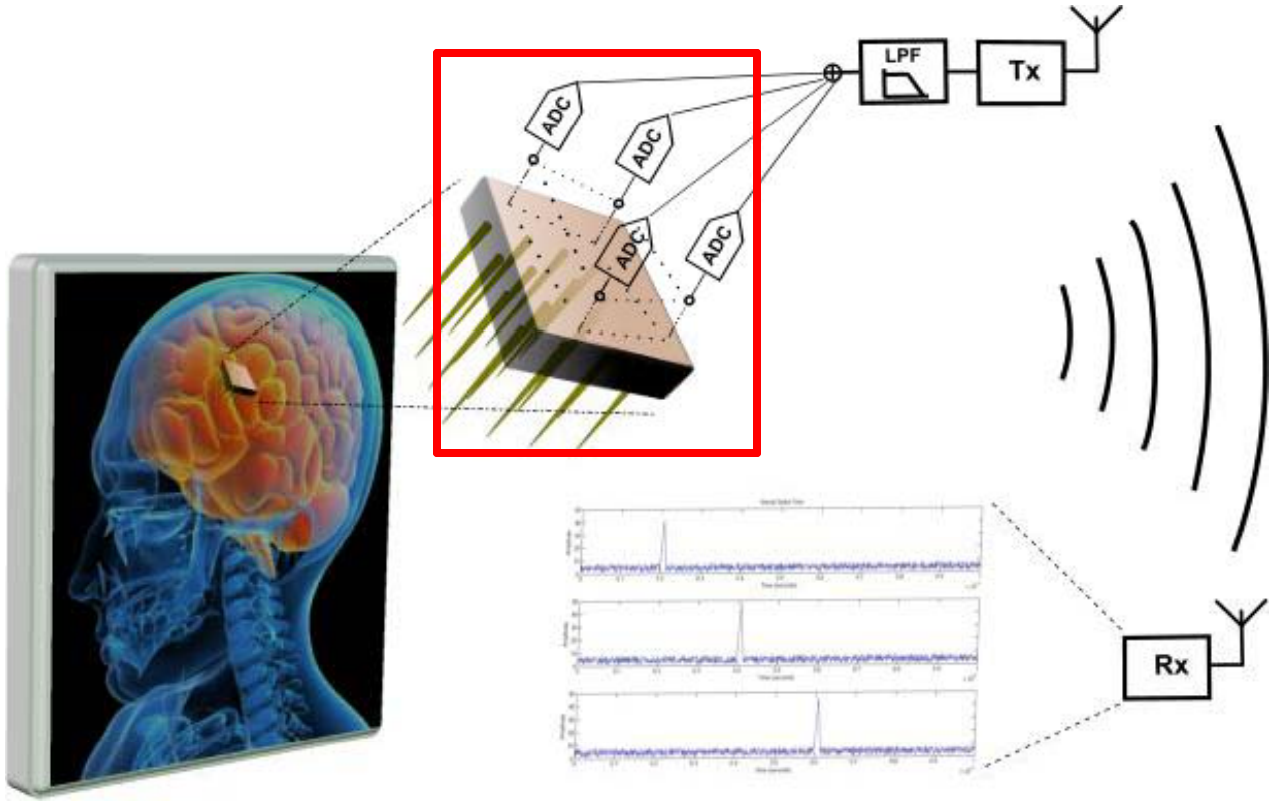
Asynchronous Compressive Sensing Front-end

Motivation

- Next-generation wireless medical sensing systems
  - Reliable: Real-time monitoring and operation
  - Portable: Miniaturized implementation
  - Low-power: Ultra-high power efficiency
- Example: wireless body area network, MIR, ECG, etc.

Neural Recordings Example

- Multi-channel neural-spike recordings



# of channels

- Routing complexity
- Power consumption

Low SNR in this app is the main limitation

Specifications

- Specifications for next-generation body area network [1]

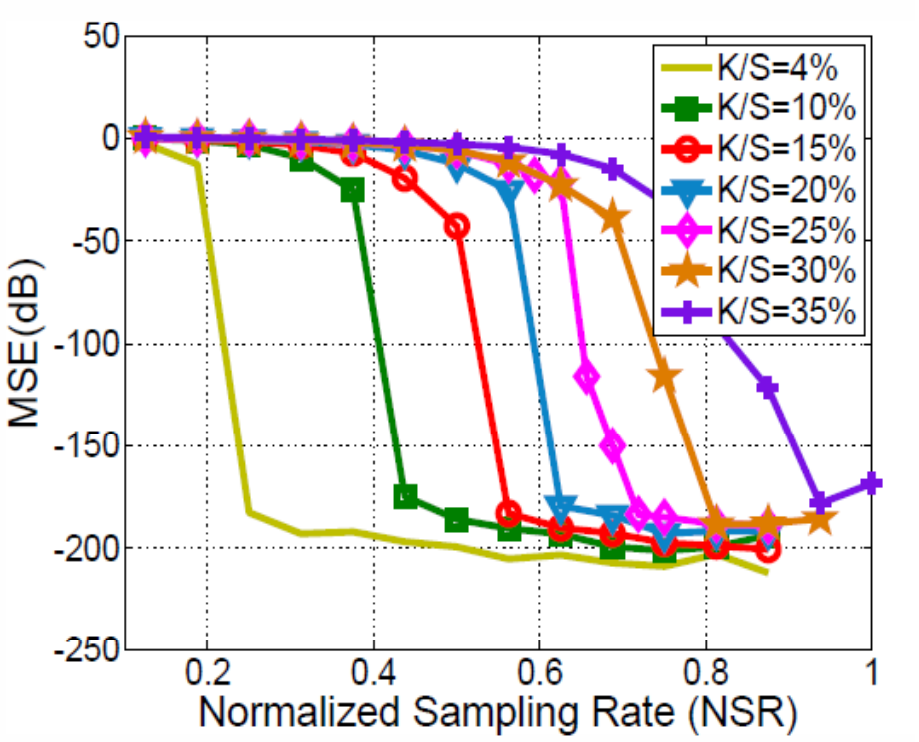
Distance	2 m standard / 5 m special use
Piconet density	2 – 4 nets / m^2
Devices per network	Max: 100
Net network throughput	Max: 100 Mbit/s
Power consumption	**~ 1 mW/Mbps**
Latency	10 ms

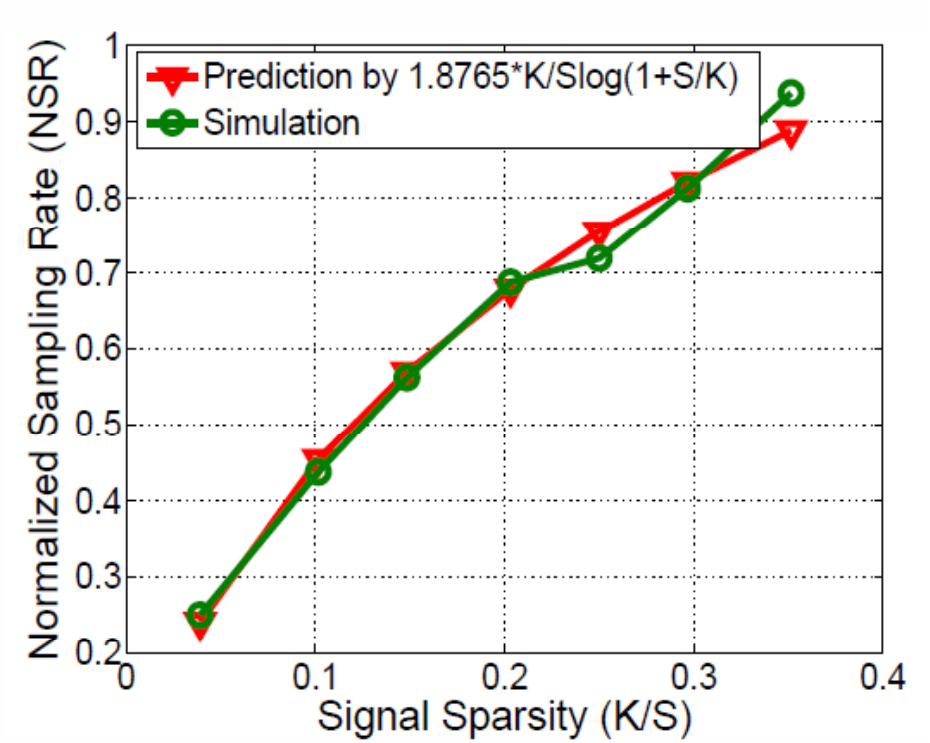
How CS Fits into This Application?

- Sub-Nyquist signal processing via Compressive Sensing (CS) ([2], [3])
  - Naturally existed sparse/compressible signals:
    - Images, videos (wavelet-domain sparse);
    - UWB pulse trainings (time-domain sparse);
    - Frequency usage (frequency-domain sparse);
  - Compressive sensing theorem states sparse and/or compressive signals can be captured at its information rate which is usually much lower than the Nyquist rate.

Performance

- Sub-Nyquist rate sampling and reconstruction



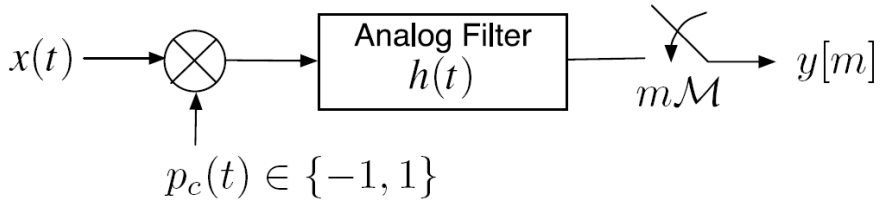


$$MSE = \frac{\|\mathbf{a} - \hat{\mathbf{a}}\|_2^2}{\|\mathbf{a}\|_2^2}$$

$$NSR = \frac{f_{Nq}}{f_{CS}} = \frac{MN}{S}$$

Architectures

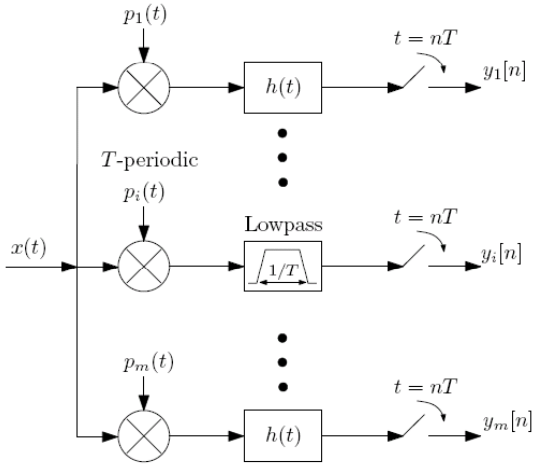
- Conventional mixed-signal CS front-end
  - Random demodulation ([4])



  - Modulated Wideband Converter ([5]

    - # of channels ≥ 4*# of bands, which is huge in terms of implementation.
    - Challenging in generating the T-periodic waveforms.

- Lacks flexibility
- Requires dedicated analog devices

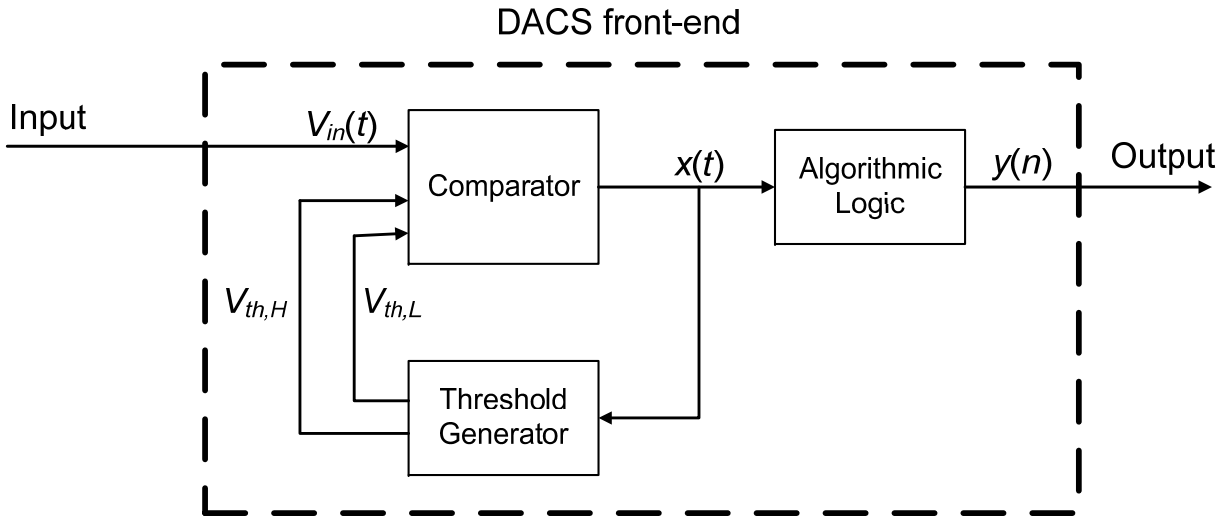


Objective

- Optimal combination of analog and digital subsystems for mixed-signal CS front-end with **low power, low complexity, and high flexibility**

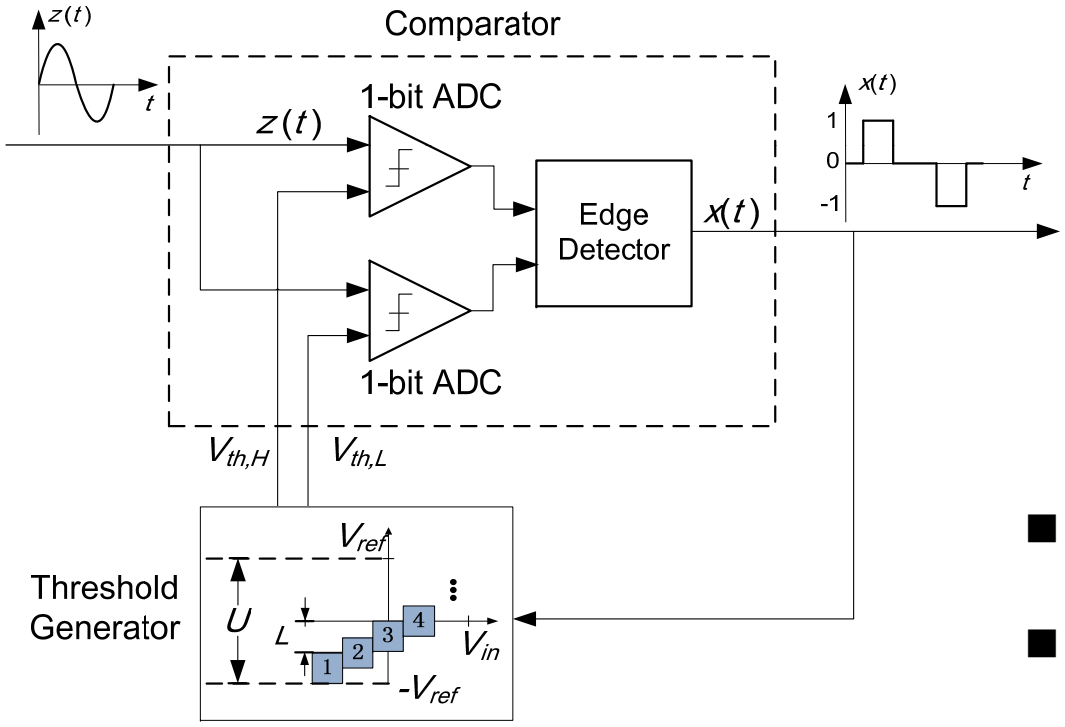
DACS front-end

- Real bio-signals are continuous and have bounded variation
  - Modulate amplitude variation to ternary timing information Digitally-assisted CS
  - **Area, power and linearity!**



DACS front-end

- Continuous-Time Ternary Encoding(CT-TE)

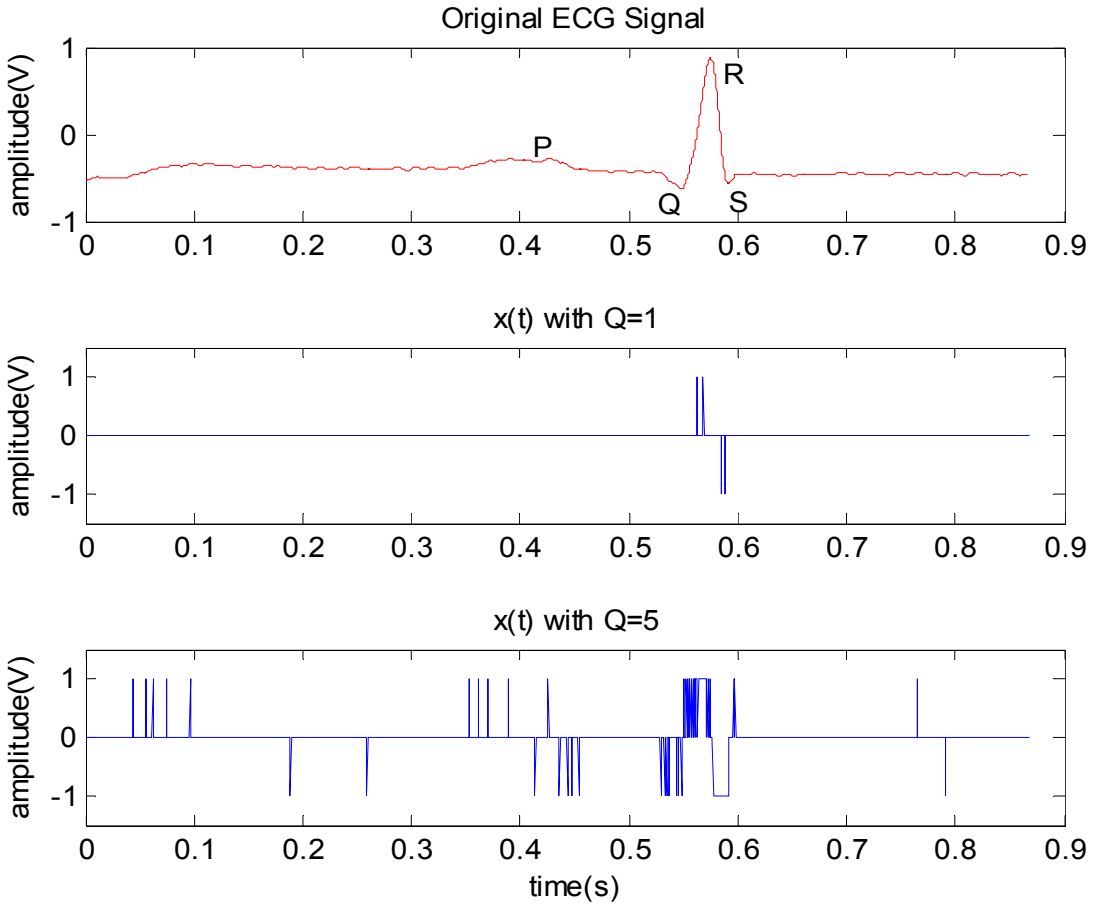


CT-TE scheme tracks input variation and modulates it to ternary timing information

- Resolution is adjustable by quantization bits *Q*
- Embedded Schmitt trigger structure is robust to noise

Resembles Delta-Sigma Modulation!

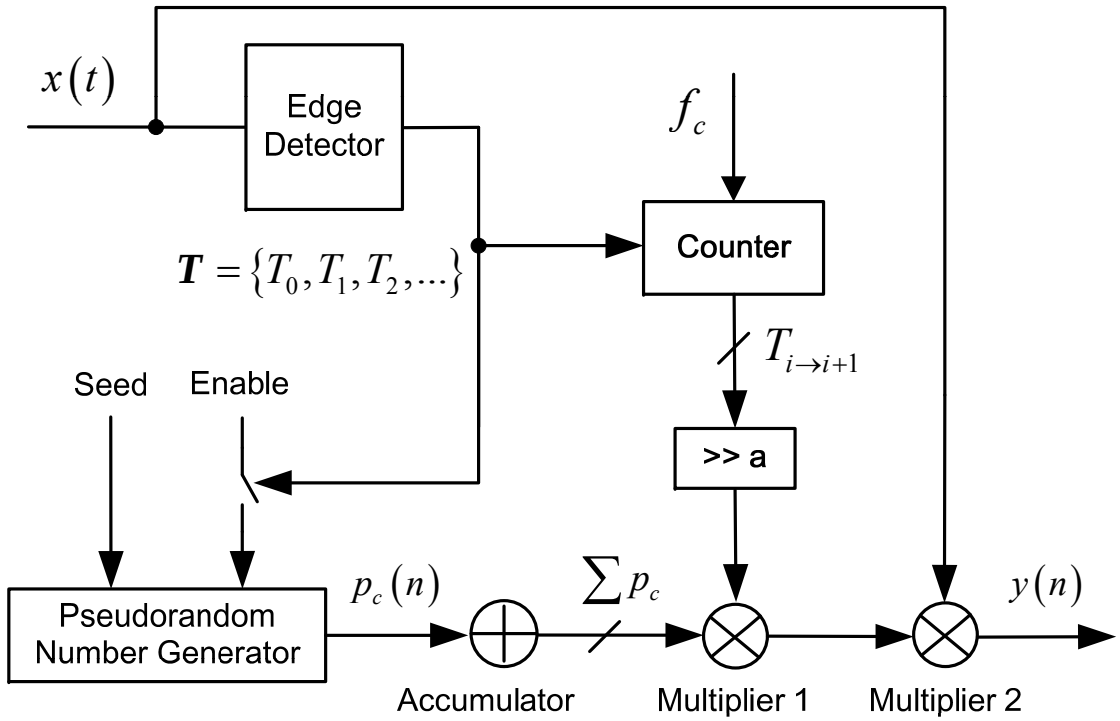
Signals



An example on ECG signal. From top to bottom, the three waveforms show original ECG signal, output of CT-TE scheme with Q = 1 and output with Q = 5, respectively.

Architecture

- Algorithmic Logic



Compressive sensing measurement generation

Calculation is trivial when input equals to 0

Part-time operation
Power saving!

Proposed *S*-member group-based total variation

- Sparse recovery via total variation

$$\min_x \alpha TV(x) + \gamma GTV(x,S) + \|y - Ax\|_2^2$$

$$TV(x) = \|Dx\|_1$$

$$GTV(x,S) = \sum_{i=1}^{N} \left\| Dx_i^{i+S_i-1} \right\|_1$$

Include both intra-group and inter-group total variation

$$S_i = \min(S, g_i)$$

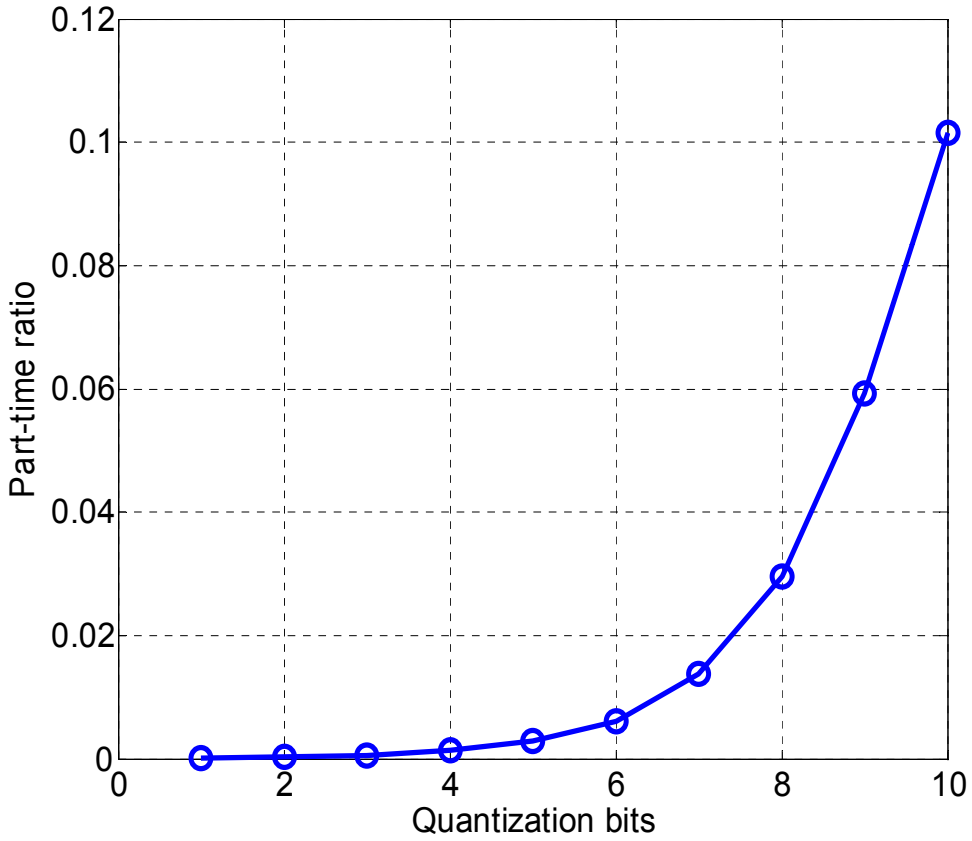
$$g_i = \arg\max_g \left(\left\| Dx_i^{i+g} \right\|_\infty \le TH < \left\| Dx_i^{i+g+1} \right\|_\infty \right)$$

- Problem finds optimal solution to equivalent compact signal

Proposed *S*-member group-based total variation

- Recovery of original ternary timing information
  - Rounding: all piecewise-constant sections have integral values.
  - If piecewise-constant value **equal** to 1 or -1, keep it same.
  - If piecewise-constant value **larger** than 1 or **smaller** than -1, there is a zero-valued section ahead current constant section. The amplitude of current section indicates the length of zero-valued section.

Simulations



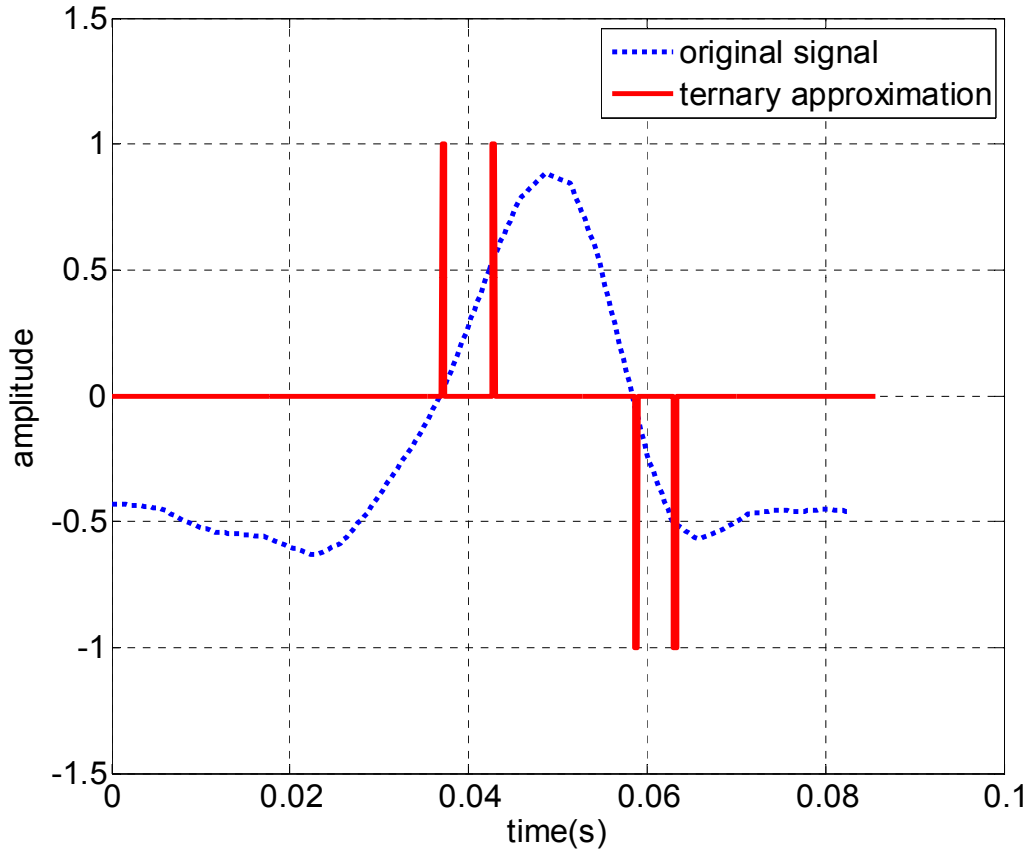
•Relationship between part-time ratio and quantization bits for ECG signal.

$$r_{\text{part-time}} = \frac{\sum_{i \in x_{\text{eq}}} T_{i \to i+1}}{\sum_{i \in x} T_{i \to i+1}}$$

Part-time ratio shows how much operating time can be saved by using proposed digitally-assisted scheme.

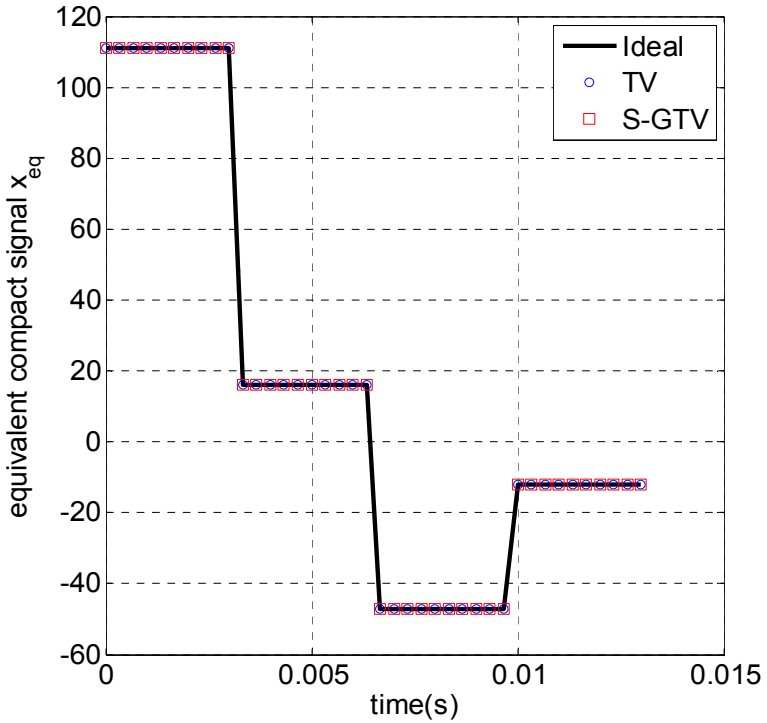
90% when Q = 10

Simulations

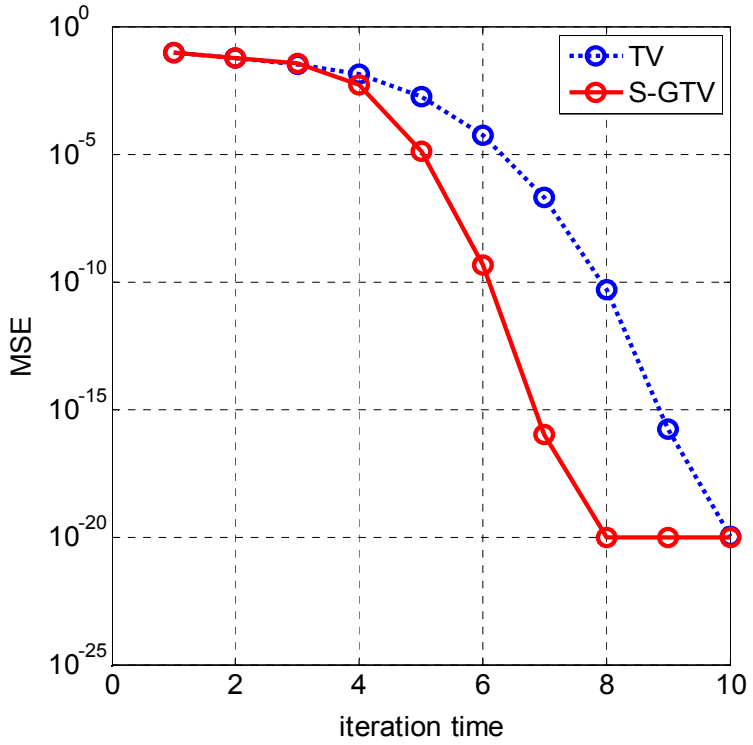


•Original waveform of QRS complex and its ternary timing approximation by CT-TE scheme, $Q = 1$.

Simulations



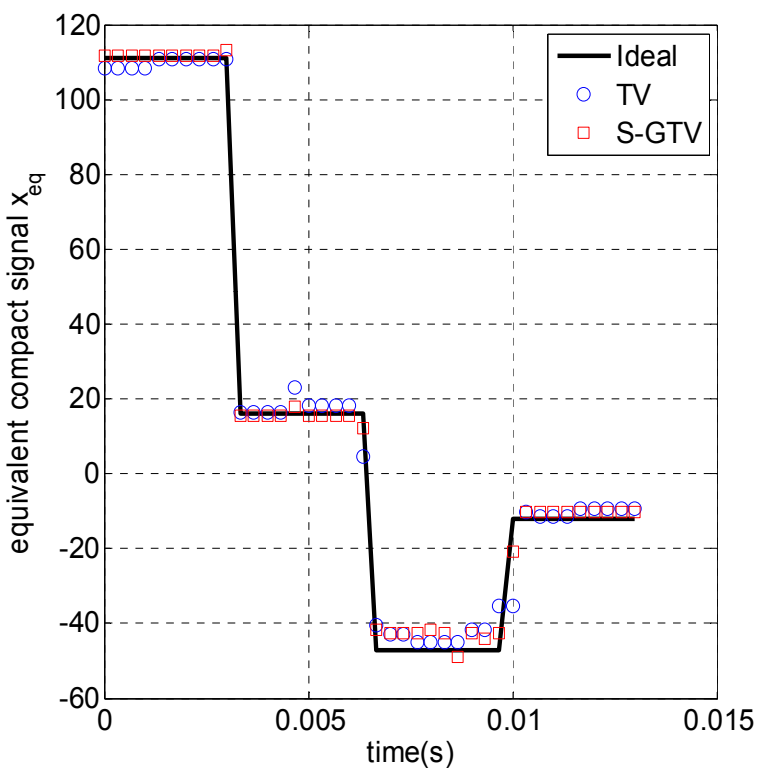
(a)



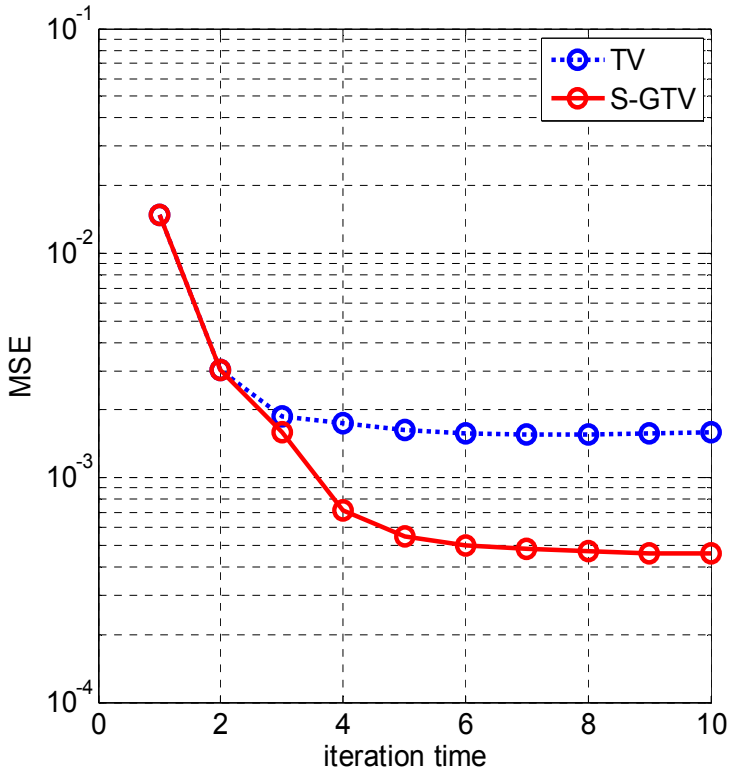
(b)

•Recovery of equivalent compact signal $x_{eq}(n)$ by conventional TV-based method and S-GTV scheme in noise-free case. (a) Recovery waveforms; (b) MSE versus iteration time.

Simulations



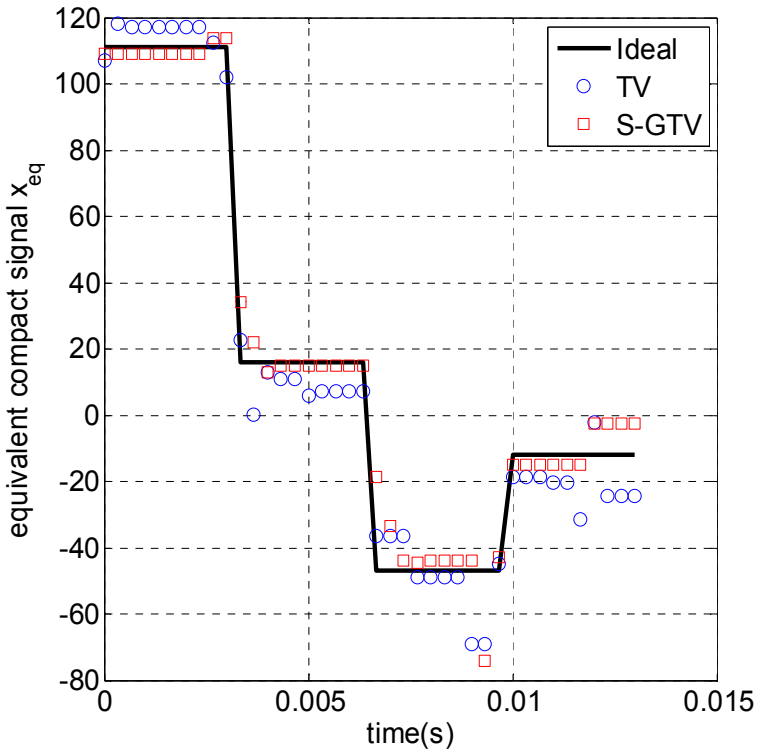
(a)



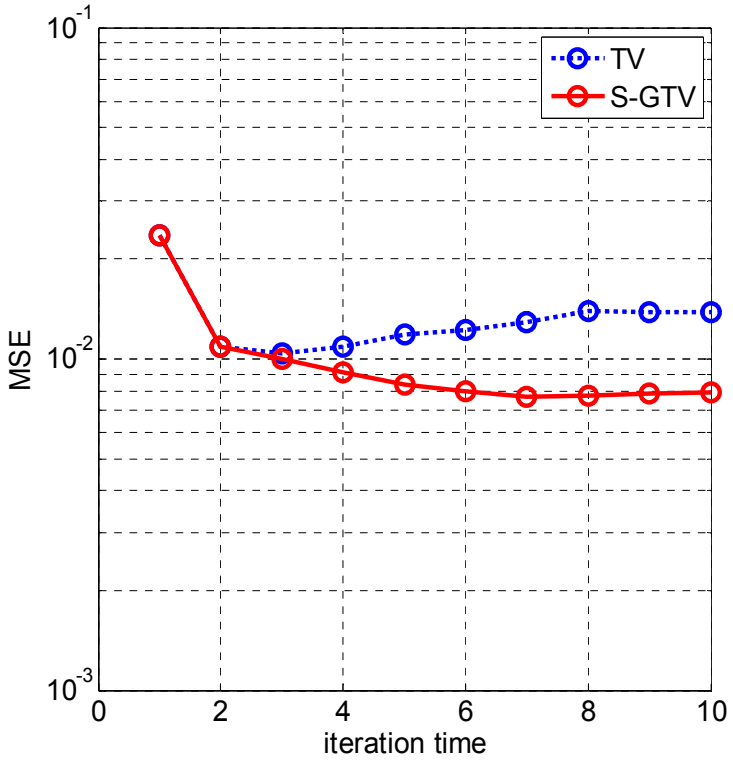
(b)

•Recovery of equivalent compact signal $x_{eq}(n)$ by conventional TV-based method and S-GTV scheme when SNR = 40dB. (a) Recovery waveforms; (b) MSE versus iteration time.

Simulations



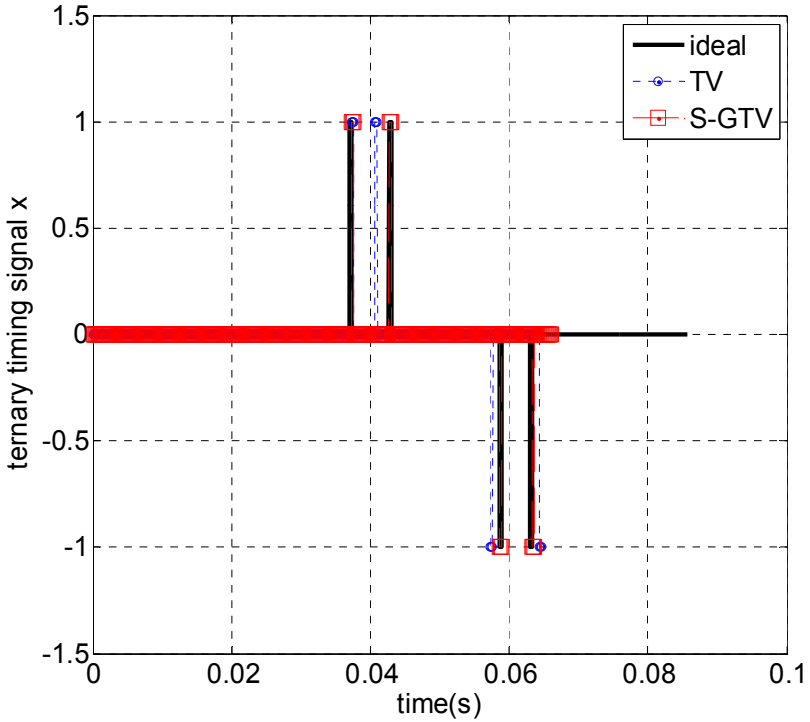
(a)

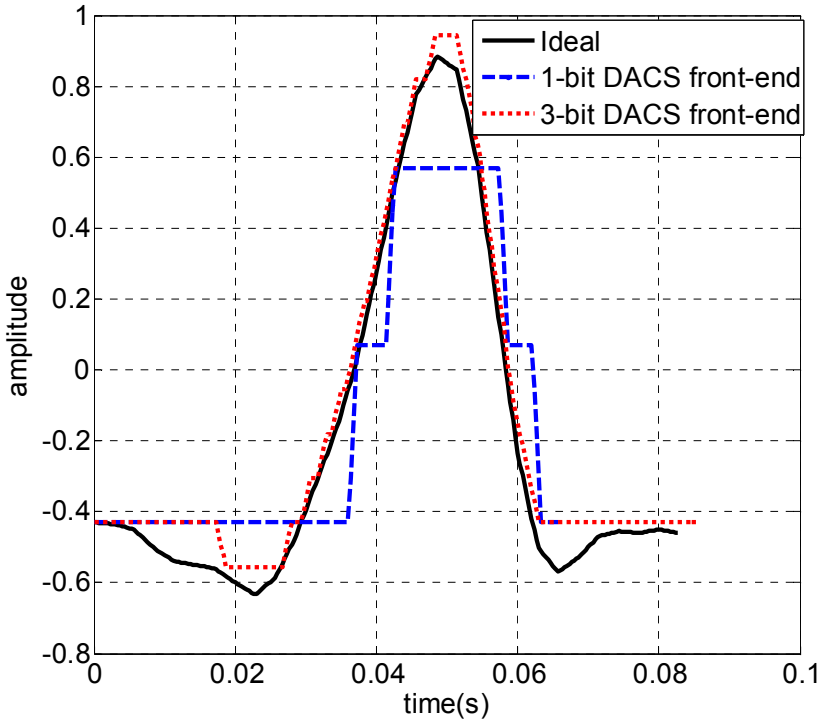


(b)

•Recovery of equivalent compact signal $x_{eq}(n)$ by conventional TV-based method and S-GTV scheme when SNR = 20dB. (a) Recovery waveforms; (b) MSE versus iteration time.

Simulations



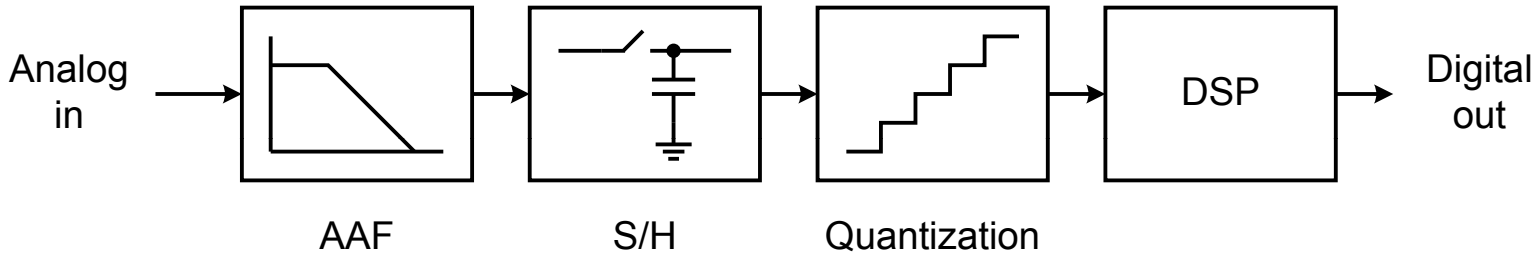


•Recovery of original ternary timing signal with rounding, SNR=20dB

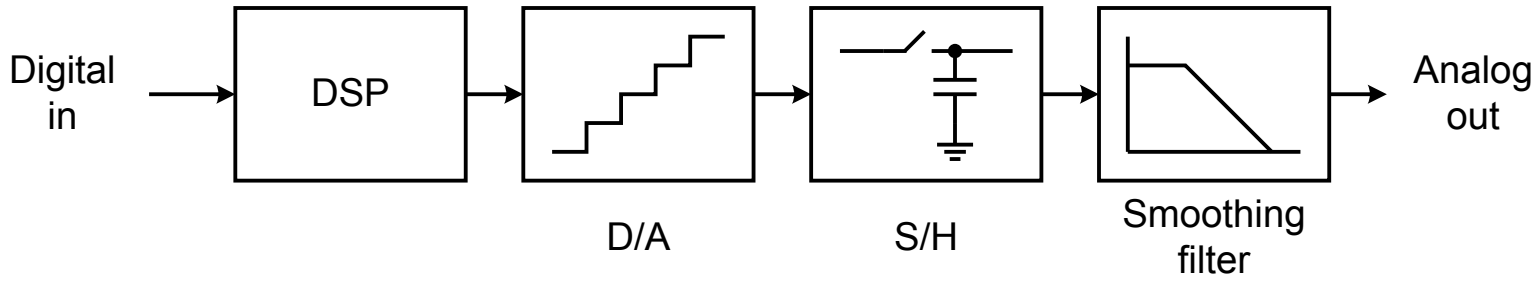
Analog to Digital Converter

A/D and D/A Conversion

A/D Conversion



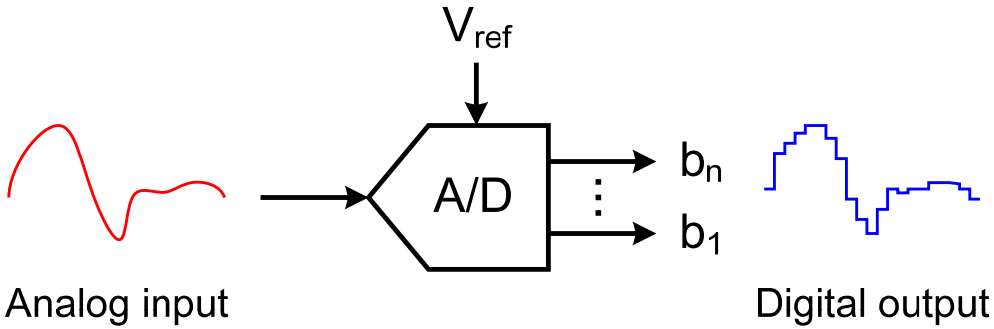
D/A Conversion



A/D and D/A Performance Metrics

- Dynamic performance
  - Signal-to-noise ratio (SNR)
  - Signal-to-noise plus distortion ratio (SNDR)
  - Spurious-free dynamic range (SFDR)
  - Aperture uncertainty
  - Dynamic range (DR)
  - Idle channel noise
- Static performance
  - Monotonicity
  - Offset
  - Gain error
  - Differential nonlinearity (DNL)
  - Integral nonlinearity (INL)

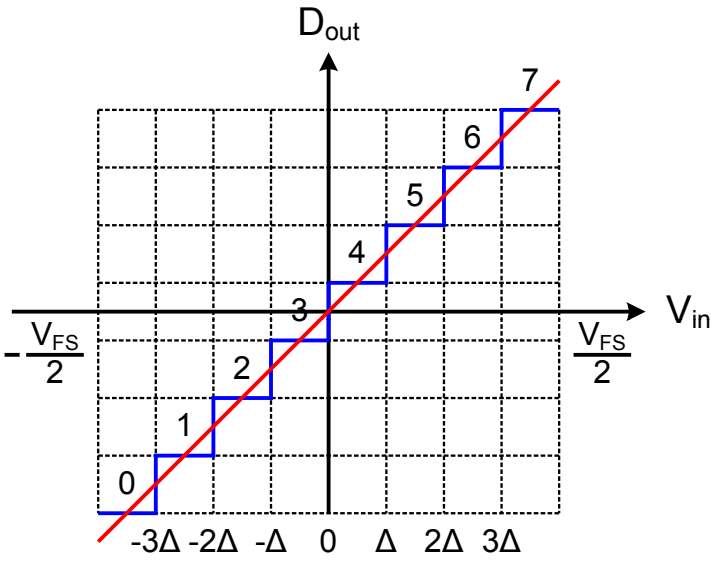
Quantization



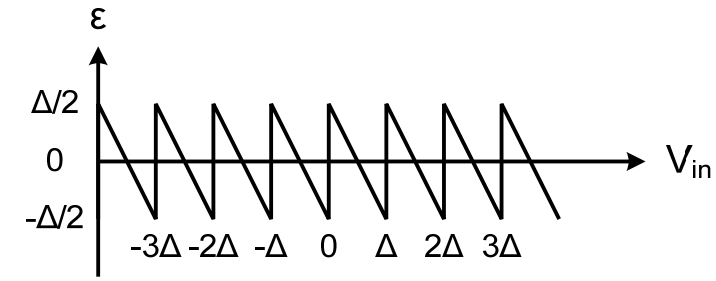
$$\underline{\text{Division}}: \quad D_{out} = \left\lfloor 2^N \cdot \frac{V_{in}}{V_{FS}} \right\rfloor$$

- Quantization = division + normalization + truncation.
- Full-scale range (V_{FS}) is determined by V_{ref}.

Quantization Error



N = 3



$$\Delta = \frac{V_{FS}}{2^N} = \text{LSB}$$

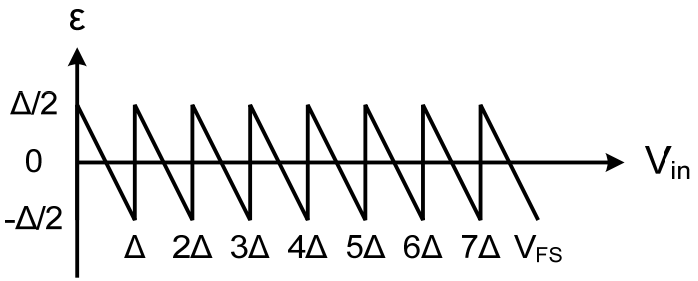
$$V_{in} \in [0, V_{FS}]$$

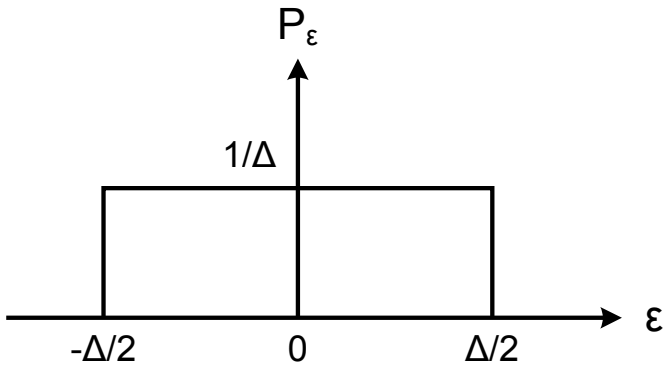
$$\varepsilon = D_{out}\Delta - V_{in} = D_{out}\left(\frac{V_{FS}}{2^N}\right) - V_{in}$$

$$-\frac{\Delta}{2} \le \varepsilon \le \frac{\Delta}{2}$$

"Random" quantization error is regarded as noise.

Quantization Noise





Assumptions:

- N is large.
- $0 \le V_{in} \le V_{FS}$ and $V_{in} >> \Delta$.
- V_{in} is active.
- ε is Uniformly distributed.
- Spectrum of ε is white.

$$\sigma_\varepsilon^{\,2} = \int_{-\Delta/2}^{\Delta/2} \varepsilon^2 \cdot \frac{1}{\Delta} \cdot d\varepsilon = \frac{\Delta^2}{12}$$

Ref: W. R. Bennett, "Spectra of quantized signals," *Bell Syst. Tech. J.*, vol. 27, pp. 446-472, July 1948.

Signal-to-Quantization Noise Ratio (SQNR)

Assume V_{in} is sinusoidal with $V_{p\text{-}p} = V_{FS}$,

$$SQNR = \frac{V_{FS}^{\ 2}/8}{\sigma_{\varepsilon}^{\ 2}} = \frac{\left(2^N \Delta\right)^2/8}{\frac{\Delta^2}{12}} = 1.5 \times 2^{2N},$$

$$\boxed{SQNR = 6.02N + 1.76dB.}$$

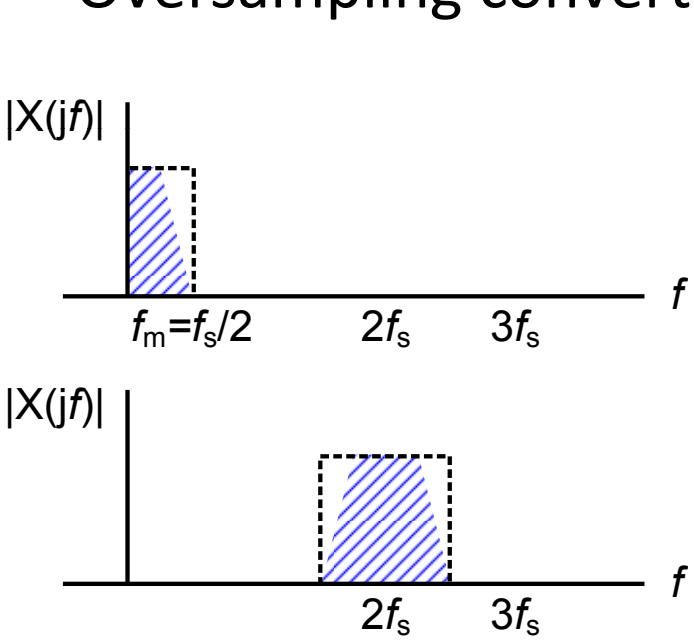
N (bits)	SQNR (dB)
8	49.9
10	62.0
12	74.0
14	86.0

- SQNR depicts the theoretical performance of an ideal ADC.
- In reality, ADC performance is limited by many other factors:
  - Electronic noise (thermal, 1/f, coupling, and etc.)
  - Distortion (measured by THD, SFDR)

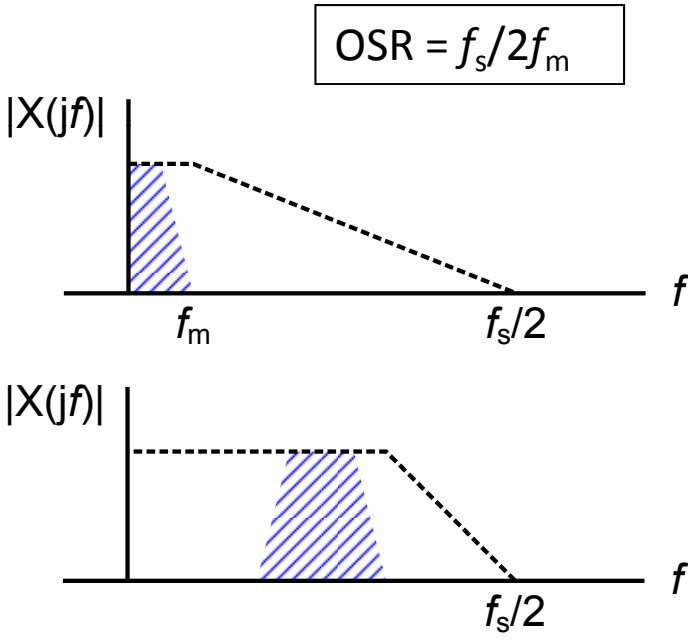
ADC Architectures

A/D Converter Architectures

- Nyquist-rate converters
- Oversampling converters



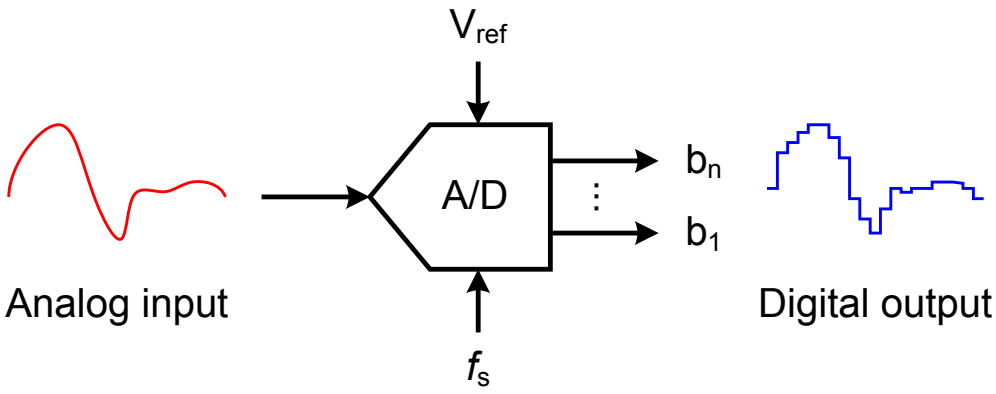
Sub-sampling



Bandpass oversampling

Nyquist-Rate ADC's

- The "black box" version of the quantization process
- Digitizes the input signal up to the Nyquist frequency ($f_s/2$)
- Minimum sampling frequency (f_s) for a given input bandwidth
- Each sample is digitized to the maximum resolution of the converter



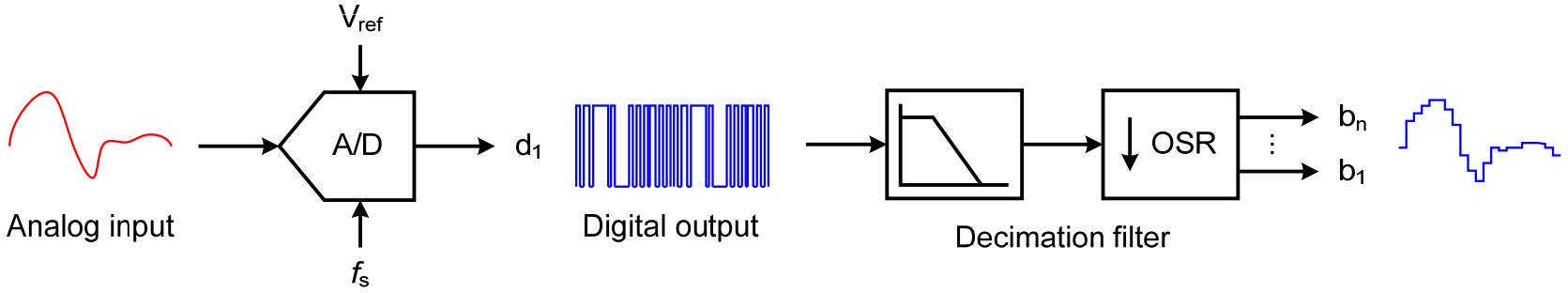
Nyquist-Rate ADC's

- Word-at-a-time (1 step)†
  - Flash
  - Folding
- Level-at-a-time (2^N steps)
  - Integration (Serial)
- Bit-at-a-time (N steps)
  - Successive approximation
  - Algorithmic (Cyclic)
- Partial word-at-a-time ($1<M\leq N$ steps)
  - Subranging
  - Multi-step
  - Pipeline

† the number in the parentheses is the "latency" of conversion, not "throughput".

Oversampling ADC's

- Sample rate is well beyond the signal bandwidth.
- Coarse quantization is combined with feedback to provide an accurate estimate of the input signal on an "average" sense.
- Quantization error in the coarse digital output can be removed by the digital decimation filter.
- The resolution/accuracy of oversampling converters is achieved in a sequence of samples ("average" sense) rather than a single sample; the usual concept of DNL and INL of Nyquist converters are not applicable.



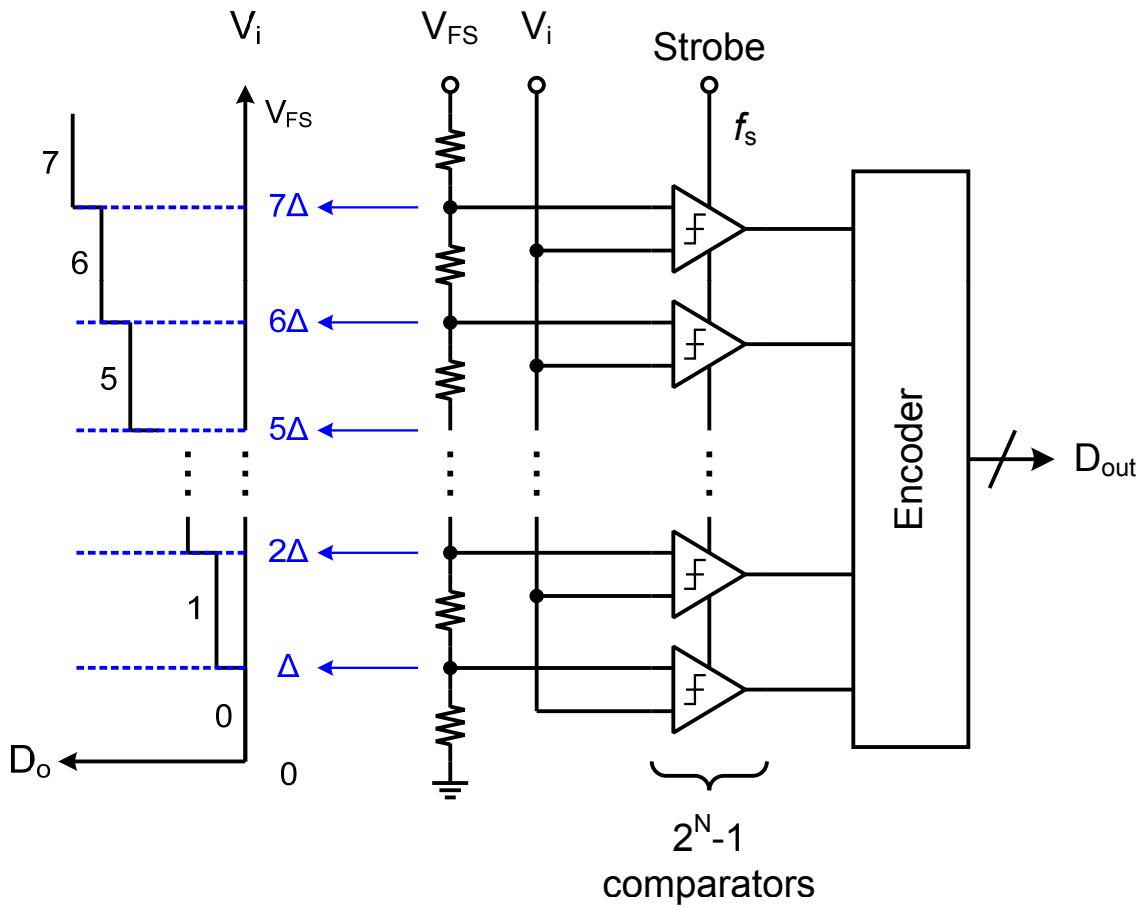
Oversampling ADC's

- Predictive
  - Delta modulation
- Noise shaping
  - Sigma-delta modulation
  - Multi-level (quantization) sigma-delta modulation
  - Multi-stage (cascaded) sigma-delta modulation (MASH)

Building Blocks for Data Converters

- Comparators (Preamp and Latch)
- Sample-and-Hold (Track-and-Hold) Amplifier
- Operational Amplifier (ELEN 474, ELEN609)
- Switched-Capacitor Amplifiers, Integrators and Filters (ELEN622)
- Voltage and Current DAC's
- Current Sources (ELEN 474)
- Voltage/Current/Bandgap References (ELEN474)

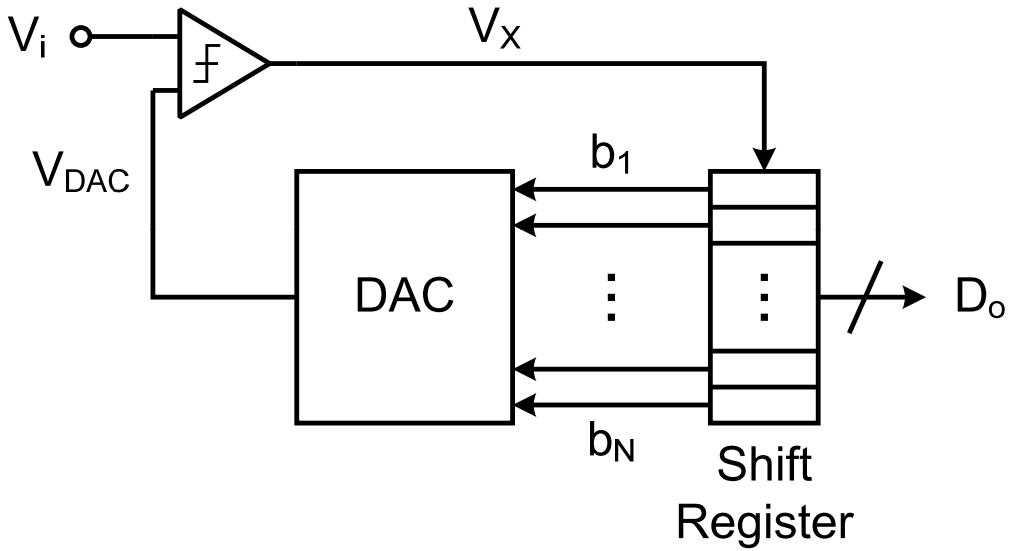
Flash ADC Architecture



- Reference ladder consists of 2^N equal size resistors
- Input is compared to 2^N-1 reference voltages.
- Massive parallelism
- Fastest ADC architecture
- Latency = 1T = $1/f_s$
- Throughput = f_s
- Complexity = 2^N

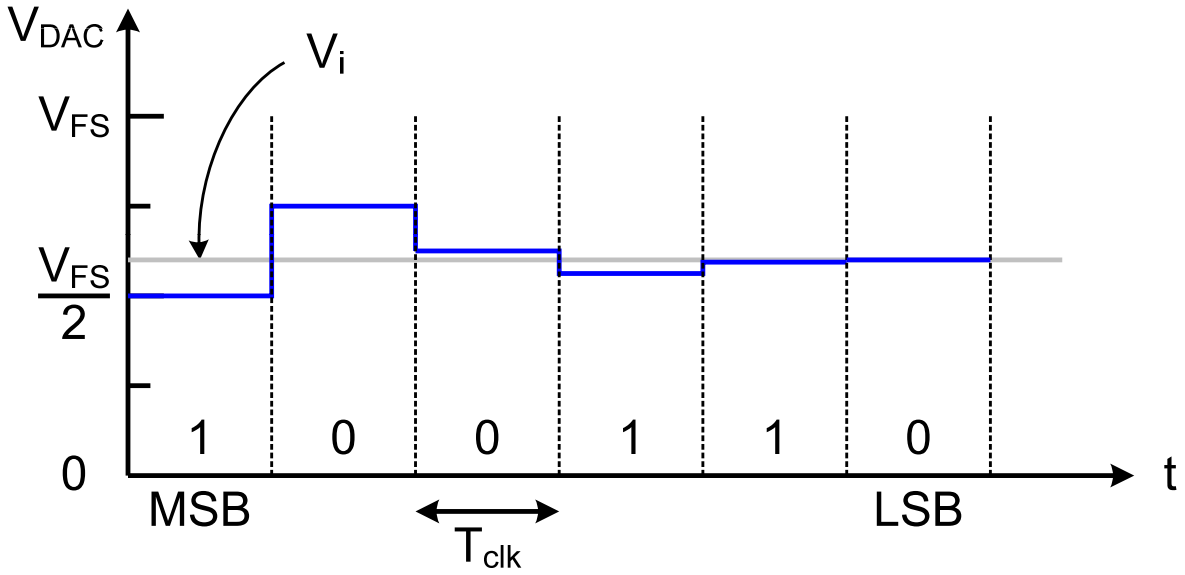
Successive Approximation ADC

Successive Approximation ADC



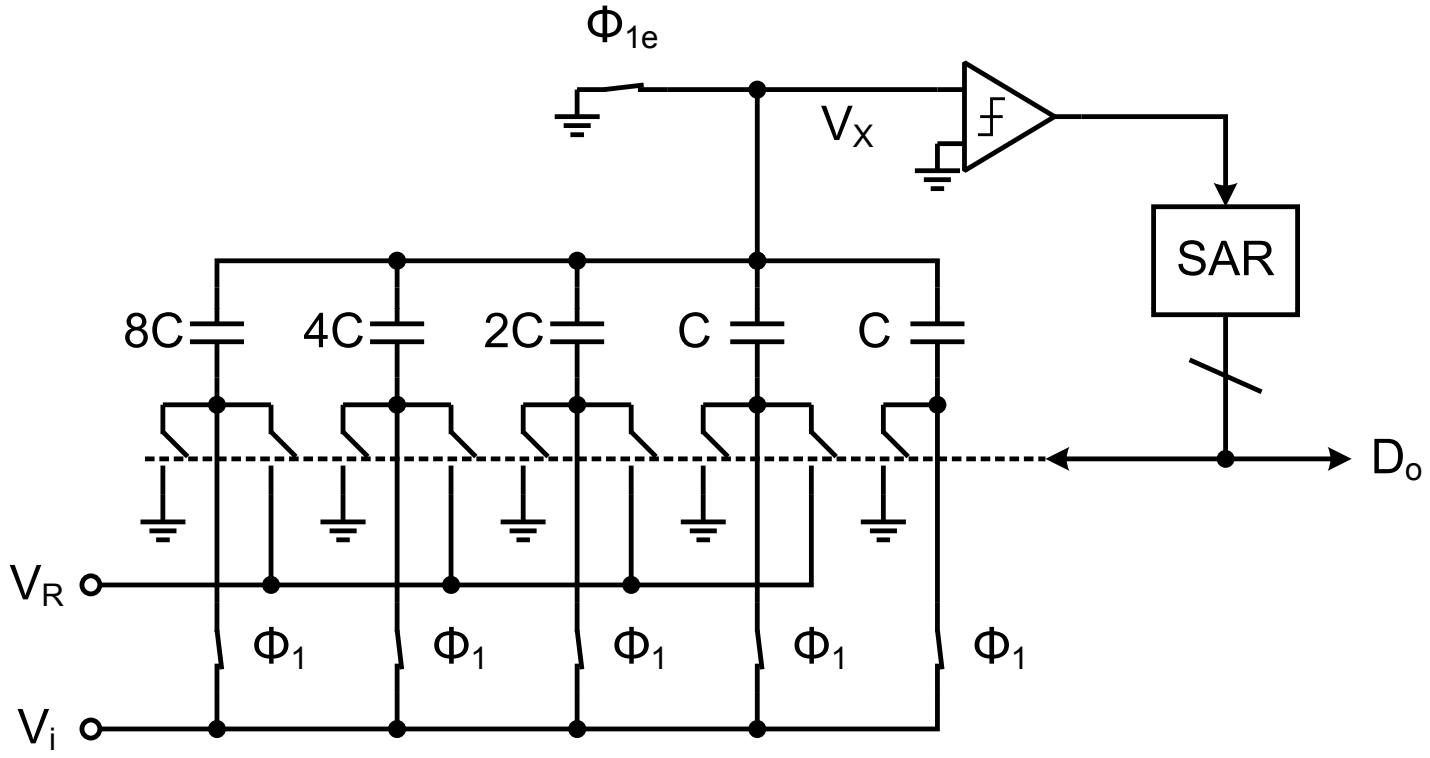
- Binary search algorithm → $N*T_{clk}$ to complete N bits.
- Conversion speed is limited by comparator, DAC, and SAR (successive approximation register)

Binary Search



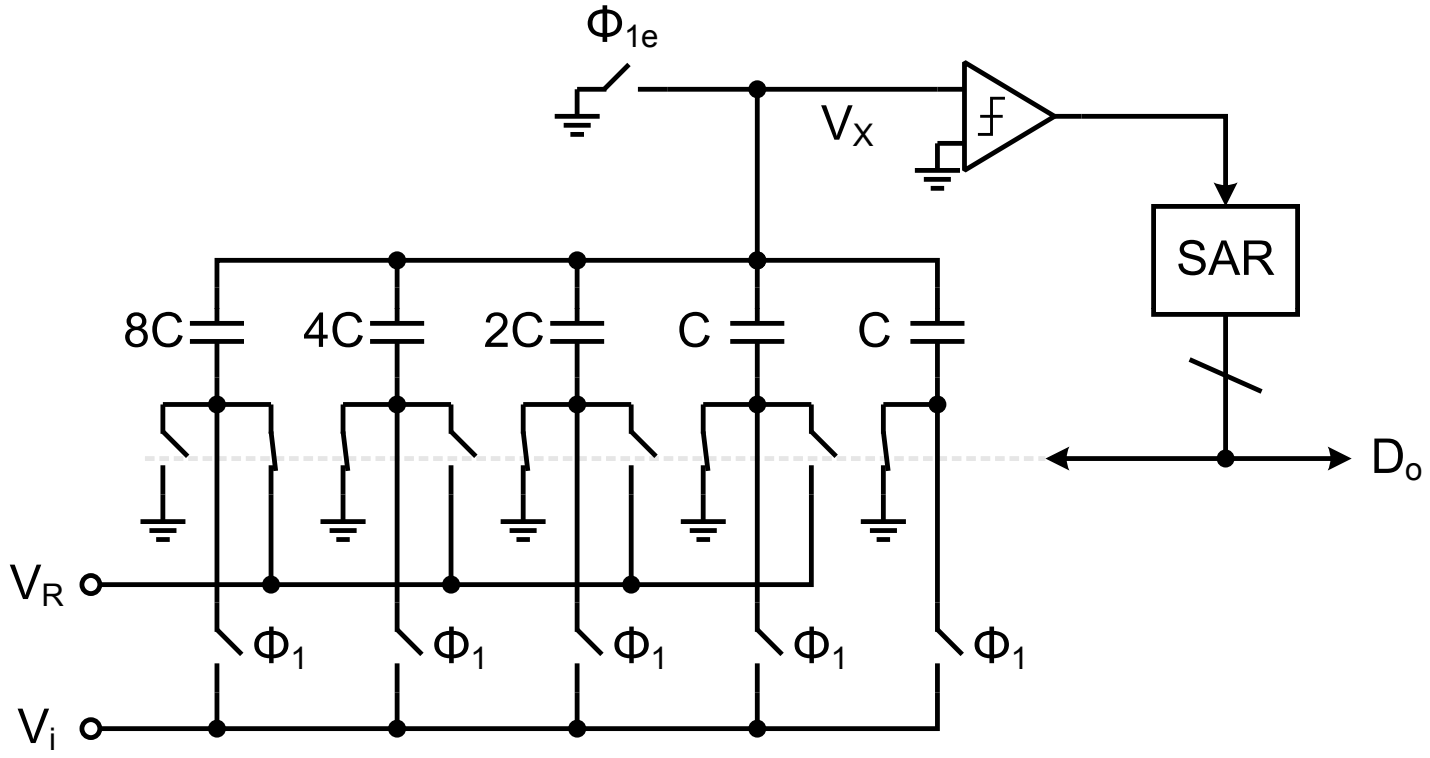
- DAC output gradually approaches the input voltage.
- Comparator differential input gradually approaches zero.

Charge Redistribution SA ADC



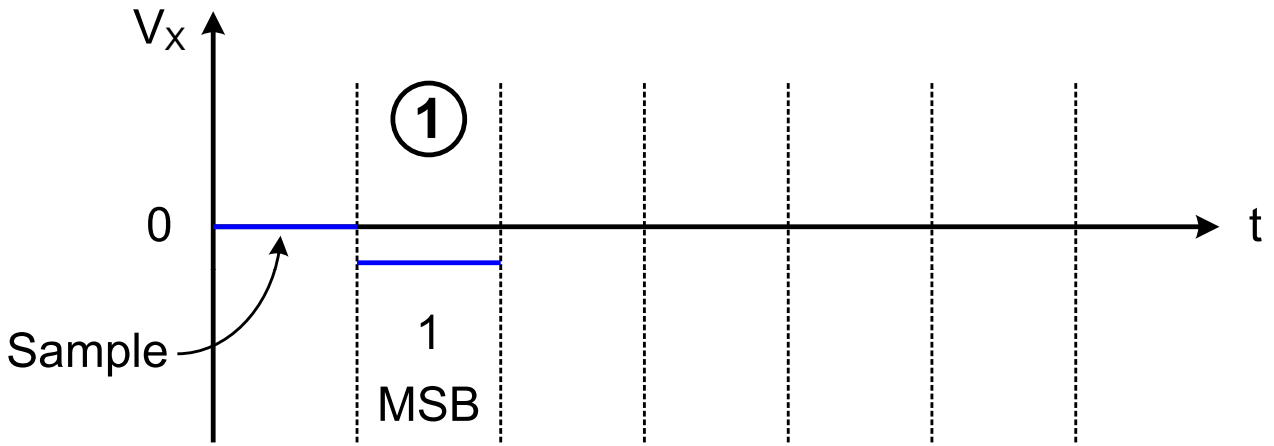
- 4-bit binary-weighted capacitor array DAC.
- Capacitor array samples input when Φ_1 is asserted (bottom-plate).

Charge Redistribution (MSB)



$$V_i \cdot \sum_{j=0}^{4} C_j = (V_R - V_X) \cdot C_4 - V_X \cdot \sum_{j=0}^{3} C_j \Rightarrow V_X = \left(V_R \cdot C_4 - V_i \cdot \sum_{j=0}^{4} C_j \right) \Big/ \sum_{j=0}^{4} C_j = \frac{V_R}{2} - V_i$$

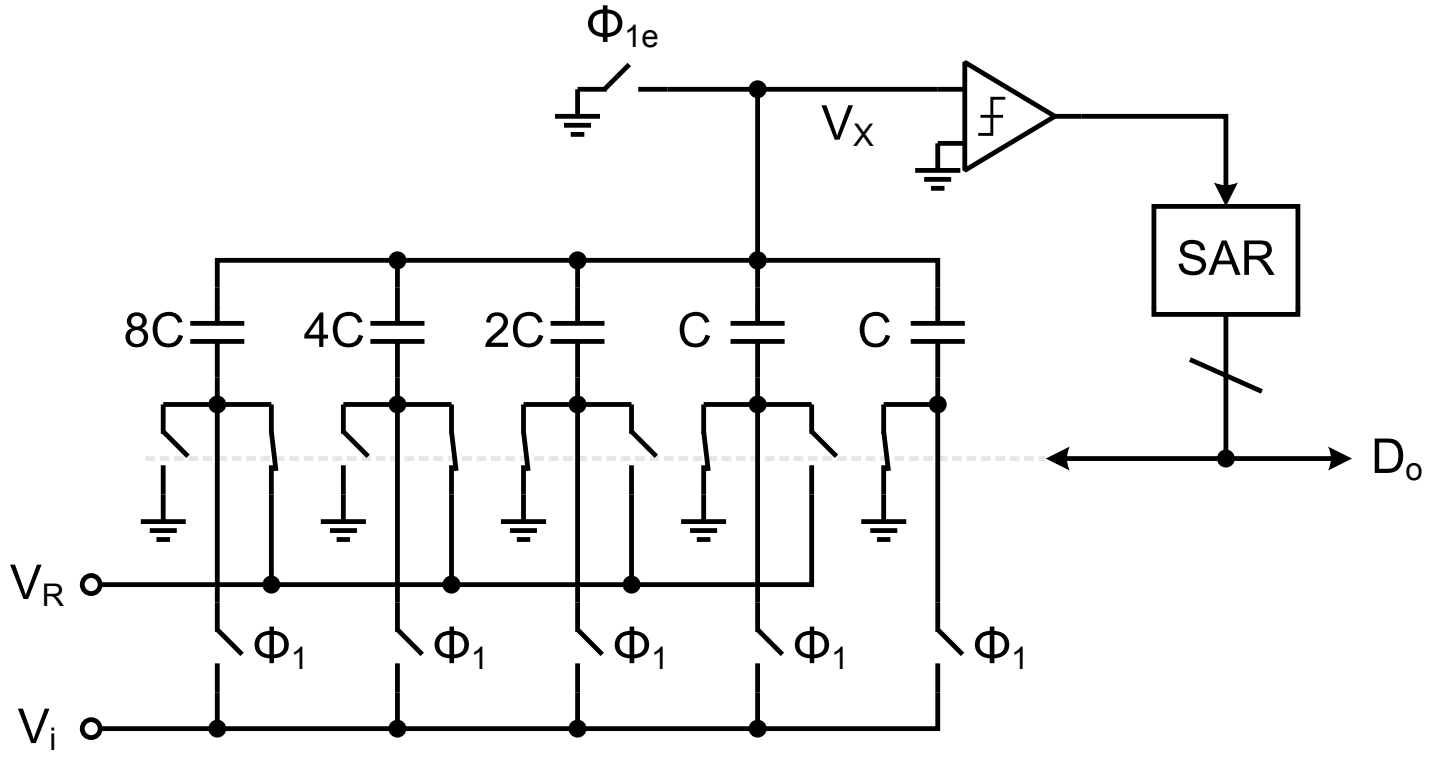
Comparison (MSB)



$$\text{MSB TEST}: V_X = \frac{V_R}{2} - V_i$$

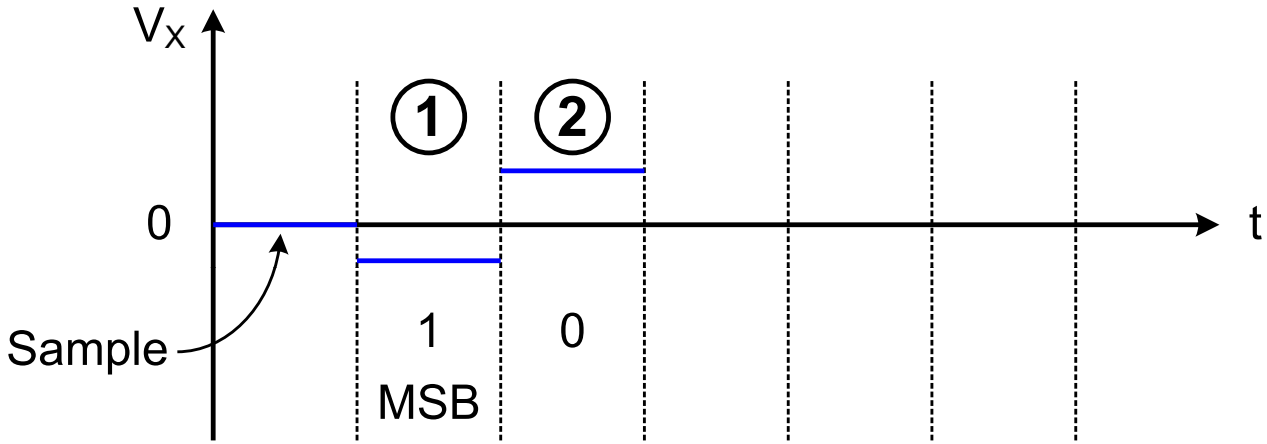
- If $V_X < 0$, then $V_i > V_R/2$, and MSB = 1, C_4 remains connected to V_R.
- If $V_X > 0$, then $V_i < V_R/2$, and MSB = 0, C_4 is switched to ground.

Charge Redistribution (MSB-1)



$$V_i \cdot 16C = (V_R - V_X) \cdot 12C - V_X \cdot 4C \Rightarrow V_X = (V_R \cdot 12C - V_i \cdot 16C)/16C = \frac{3}{4}V_R - V_i$$

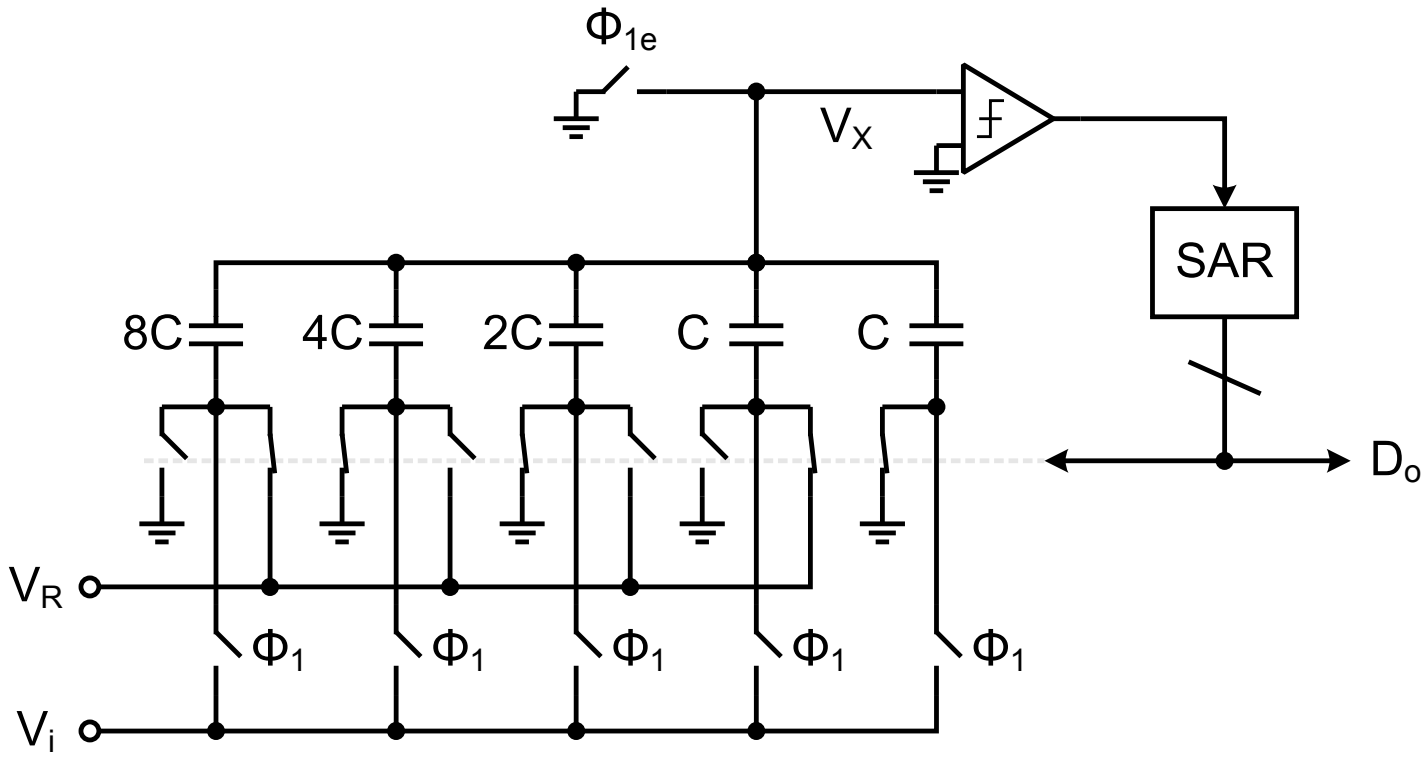
Comparison (MSB-1)



$$\text{MSB TEST}: V_X = \frac{3}{4}V_R - V_i$$

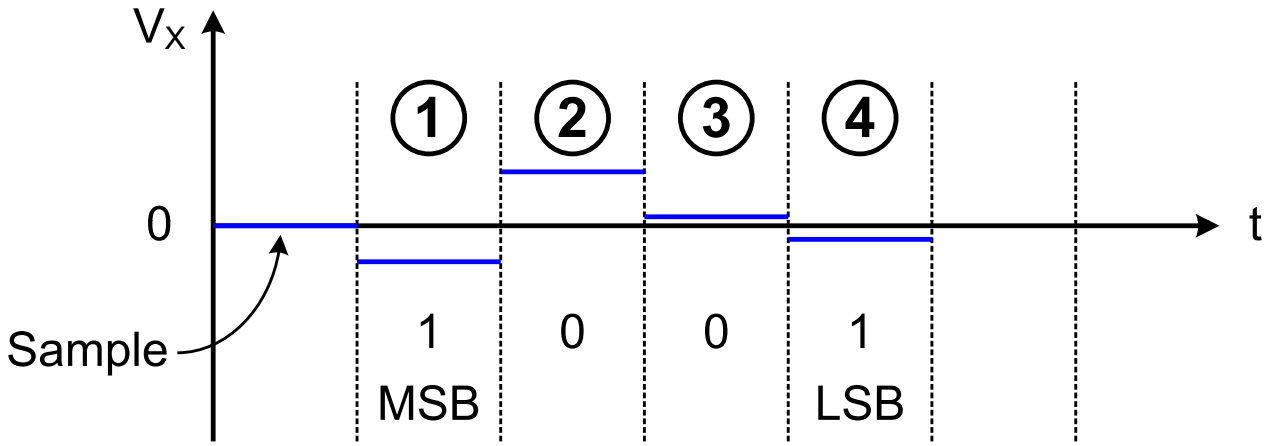
- If $V_X < 0$, then $V_i > 3V_R/4$, and MSB-1 = 1, C_3 remains connected to V_R.
- If $V_X > 0$, then $V_i < 3V_R/4$, and MSB-1 = 0, C_3 is switched to ground.

Charge Redistribution (Other Bits)



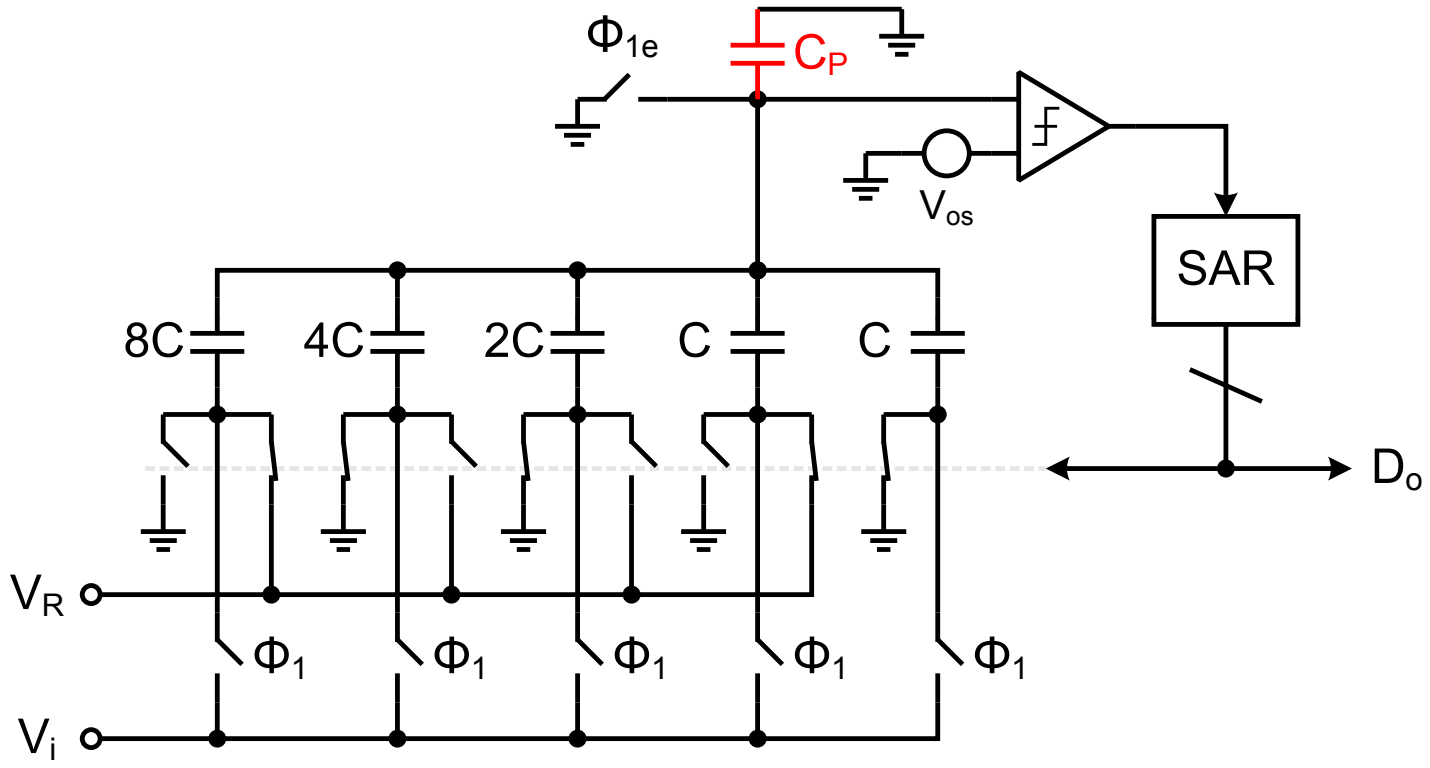
Test completes when all four bits are determined w/ four charge redistributions and comparisons.

After Four Clock Cycles…



- Usually, half T_{clk} is allocated for charge redistribution and half for comparison + digital logic.
- V_X always converges to 0 (V_{os} if comparator has nonzero offset).

Bottom-Plate Parasitics



- If $V_{os} = 0$, C_P has no effect; otherwise, C_P attenuates V_X.
- AZ can be applied to the comparator to reduce offset.

Summary on SA ADC

- Power efficiency – only comparator consumes DC power.
- DAC nonlinearity limits the INL and DNL of the SA ADC
  - N-bit precision requires N-bit matching from the cap array.
  - Calibration can be performed to remove mismatch errors (Lee, JSSC 84).
- If C_P=0, comparator offset V_{os} introduces an input-referred offset V_{os}; for nonzero C_P, input-referred offset is larger than V_{os} ($\delta \sim C_P/\Sigma C_j$).
- If V_{os}=0, CP has no effect ($V_X \rightarrow 0$ at the end of search); otherwise, charge sharing occurs at summing node (V_X is attenuated).
- Binary search is sensitive to intermediate errors made during search
  - DAC must settle into ½ LSB within the time allowed.
  - Comparator offset must be constant (no hysteresis).
  - Nonbinary search can be used (Kuttner, ISSCC, 2002).

A 6b 1.6GS/s ADC with Redundant Cycle 1-Tap Embedded DFE in 90nm CMOS

E. Zhian Tabasy, A. Shafik, S. Huang, N. Yang, S. Hoyos, and S. Palermo

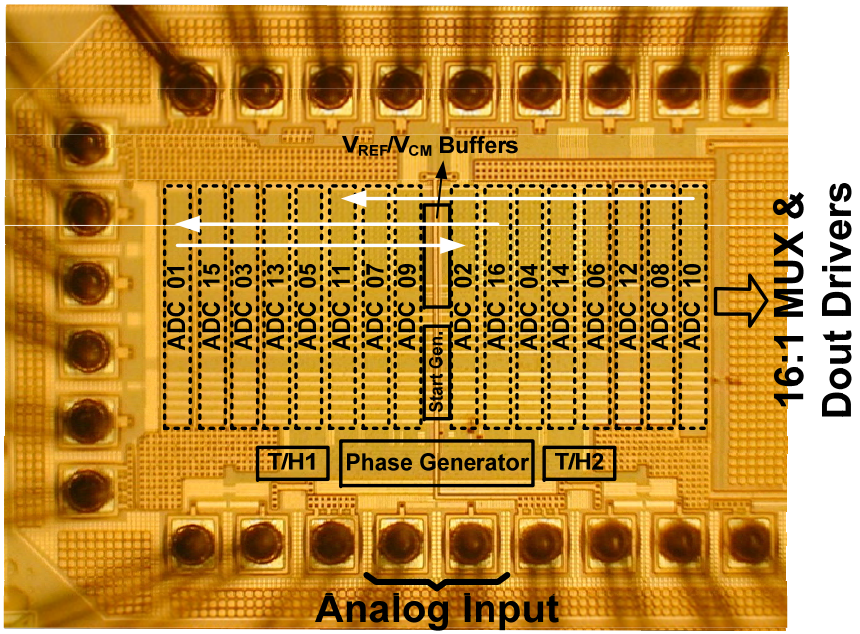


TABLE I
ADC PERFORMANCE COMPARISON

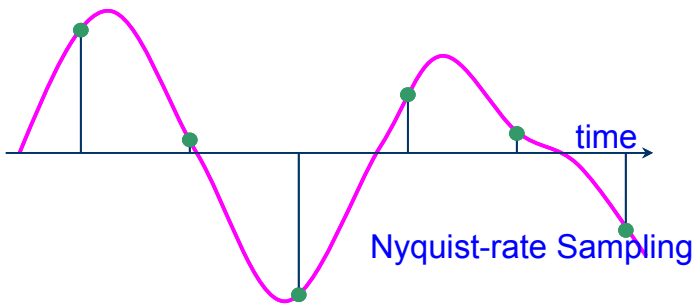
SPECIFICATION	[3]	[8]	[9]	This Work
CMOS Technology	130nm	130nm	40nm	90nm
Supply Voltage (V)	1.2	1.2	1.0	1.3
Resolution (bit)	5	6	6	6
Samp. Rate (GS/s)	4.8	1.25	1.25	1.6
ERBW (GHz)	4	0.45	0.6	0.8
Max ENOB (bit)	4.76	5.5	4.77	4.75
Power (mW)	300	32	6.08**	20.1
FoM(pJ/Conv.-Step)	2.3	0.78	0.18	0.46
Embedded Equalization	DFE*	N/A	N/A	DFE
Active Area (mm^2)	1.69	2.32	0.014	0.24

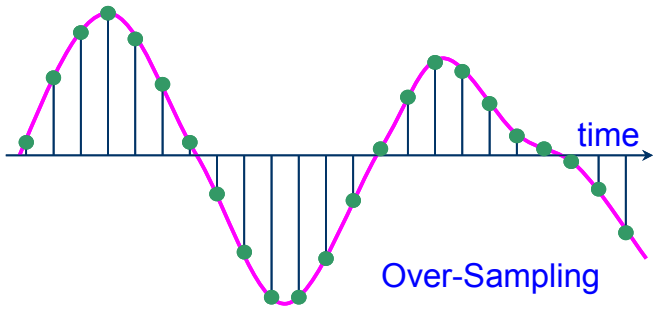
* The embedded equalization is referred as multi-level DFE in [3].
** There is no front-end active T/H, and this structure does not need reference or common-mode voltage buffers.

Oversampling ADC

Nyquist-rate Sampling and Over-Sampling

- Nyquist-rate Sampling
  - Sampling frequency F_S slightly higher than the Nyquist rate of the signal, $F_{Nyquist} = 2 \cdot f_b$.
  - $F_S > 2 \cdot f_b$ but $F_S \approx 2 \cdot f_b$.
- Over-Sampling
  - Sampling frequency F_S much higher than the Nyquist rate of the signal, $F_{Nyquist} = 2 \cdot f_b$.
  - $F_S >> 2 \cdot f_b$.
- The ratio $M = F_S/(2 \cdot f_b)$ is called oversampling ratio (OSR).





Definition:
Oversampling Ratio (OSR)

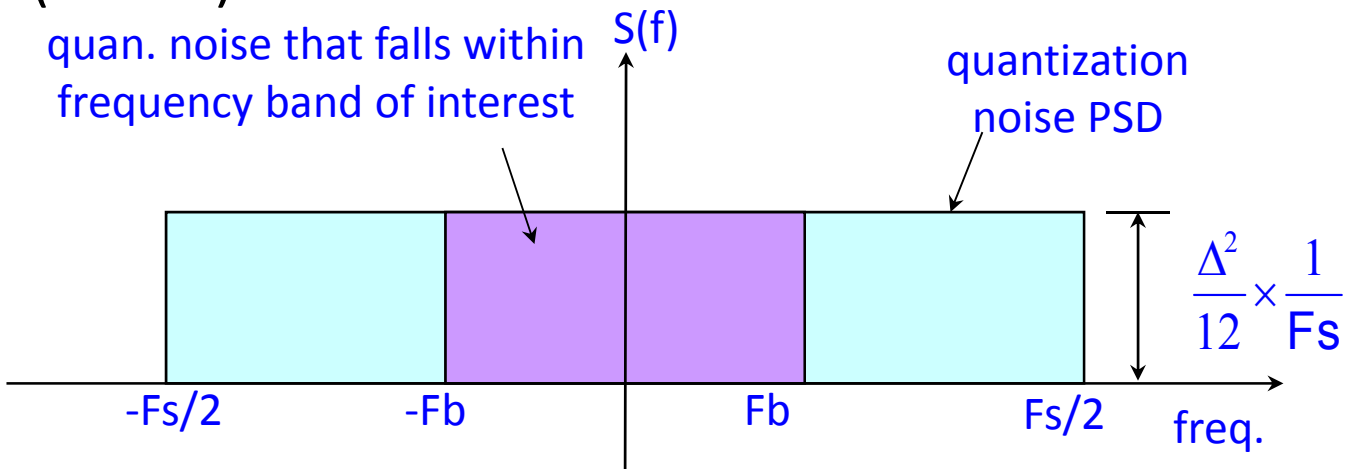
$$OSR = \frac{F_S}{2f_b}$$

Nyquist-rate and Over-sampling Data Converters

- Nyquist-rate data converters
  - Sampling frequency F_S slightly higher than the Nyquist rate of the signal, $F_{Nyquist} = 2 \cdot f_b$.
  - OSR is larger but close to 1
- Over-sampling data converters
  - Sampling frequency F_S much higher than the Nyquist rate of the signal, $F_{Nyquist} = 2 \cdot f_b$
  - OSR usually larger than 8.

Why Over-Sampling? – Better SQNR

- Benefit of over-sampling: lower quantization noise within signal bandwidth.
- Assuming quantization noise is white, every time we double the sample frequency, the effective resolution increases with 3 dB (0.5 bit).



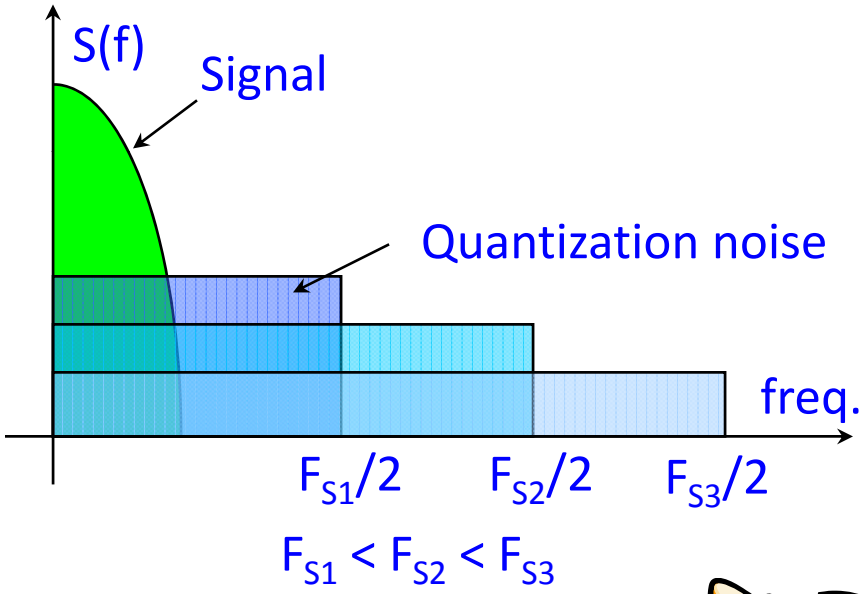
The quantization noise outside of the frequency of interest could be filtered out by post digital low pass filtering.

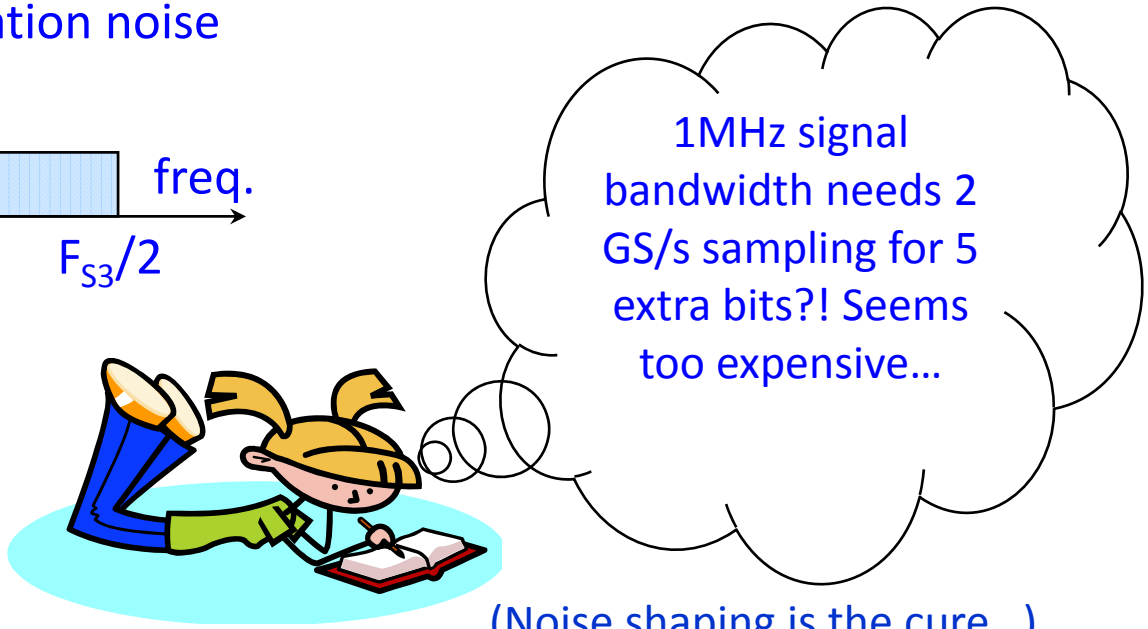
* In many situations, dither is needed to make quantization white.

Why Over-Sampling? – Better SQNR (Cont'd)

- The higher sampling frequency, the lower inband quantization noise

Doubling sampling frequency increases equivalent resolution by 3 dB.
6 bit resolution improvement means 4096 times higher clock frequency!!

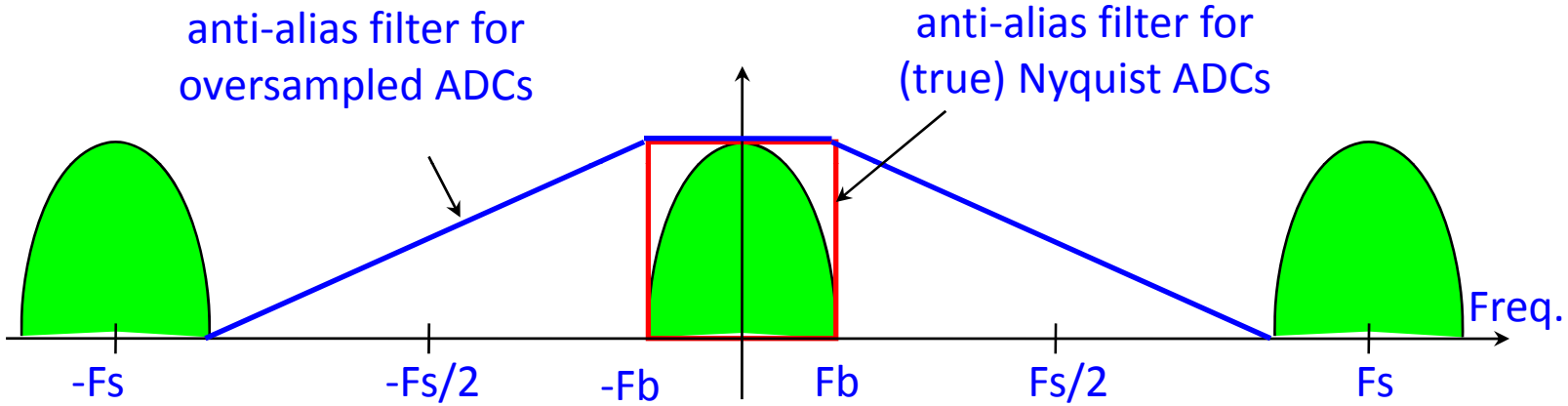




(Noise shaping is the cure…)

Why Over-Sampling? – Relaxed AAF Requirement

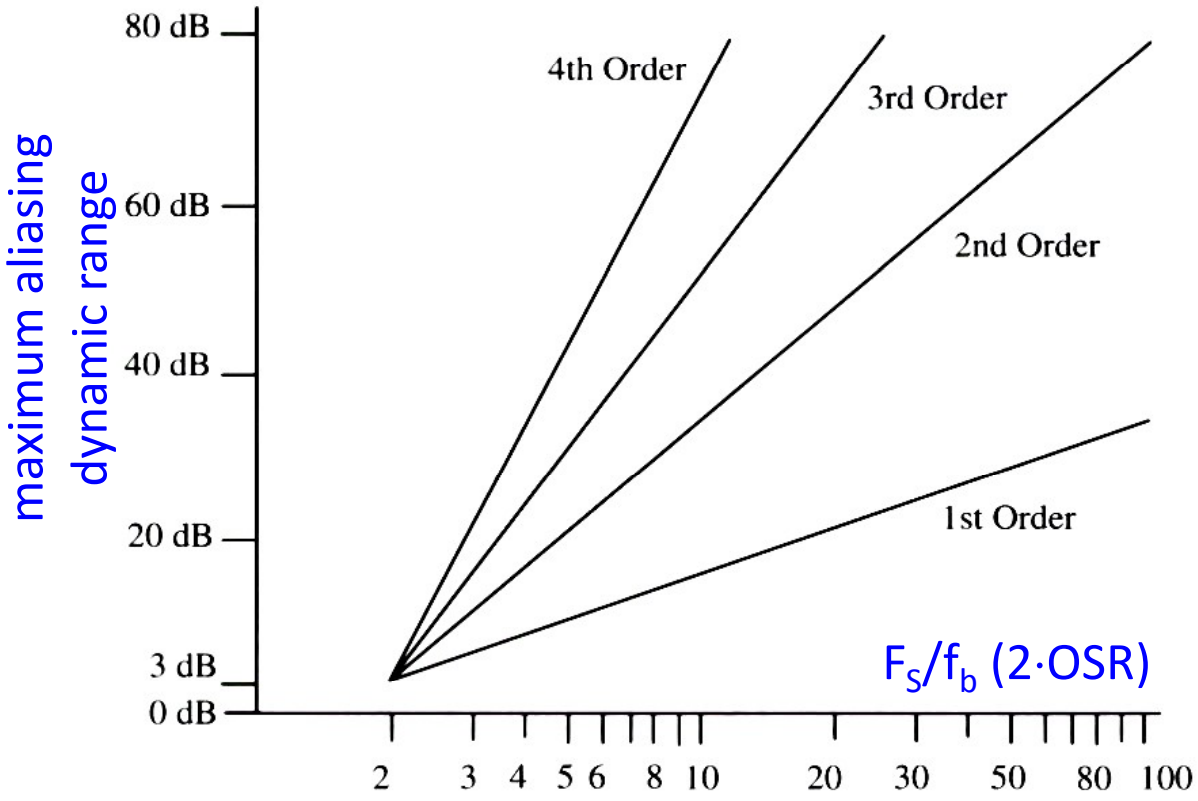
- Another benefit for oversampled A/D conversion is much relaxed anti-alias filter requirements.



- For true Nyquist rate ADCs, very steep brick wall type anti-alias filters are required with large phase distortion, high power consumption, and large silicon area.
- In practice, Nyquist rate ADCs always have certain “oversampling” with practical anti-alias filters.
- For over-sampling ADCs, simple low order anti-alias filters could be utilized.

Anti-Alias Filter Order vs. OSR

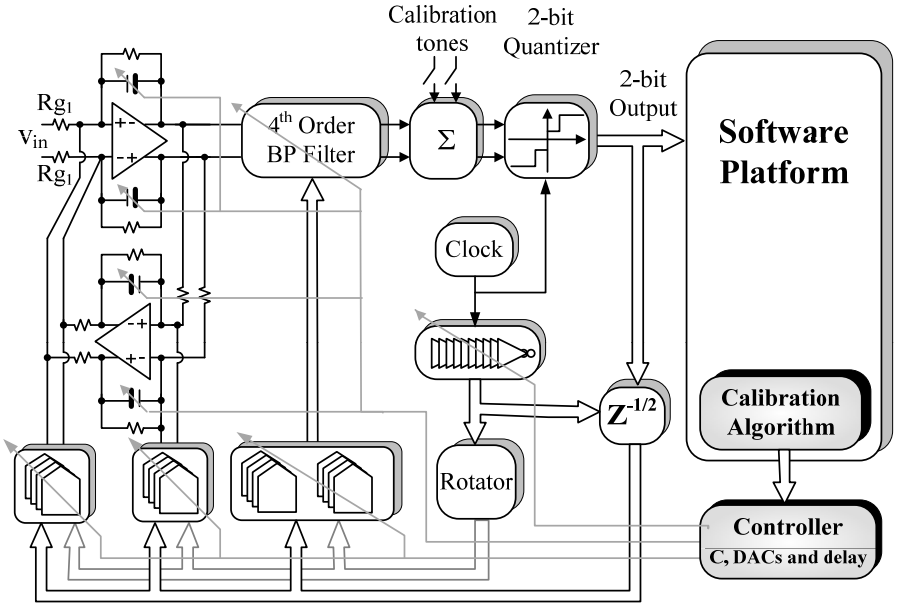
- Anti-alias filter order (Butterworth type) vs. OSR



[R. van de Plassche, CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters, 2nd ed., 2003, p. 41]

A 6th-order 200MHz IF Bandpass Sigma-Delta Modulator With over 68dB SNDR in 10MHz Bandwidth

Cho-Ying Lu, Fabian Silva-Rivas, Praveena Kode, Jose Silva-Martinez and Sebastian Hoyos



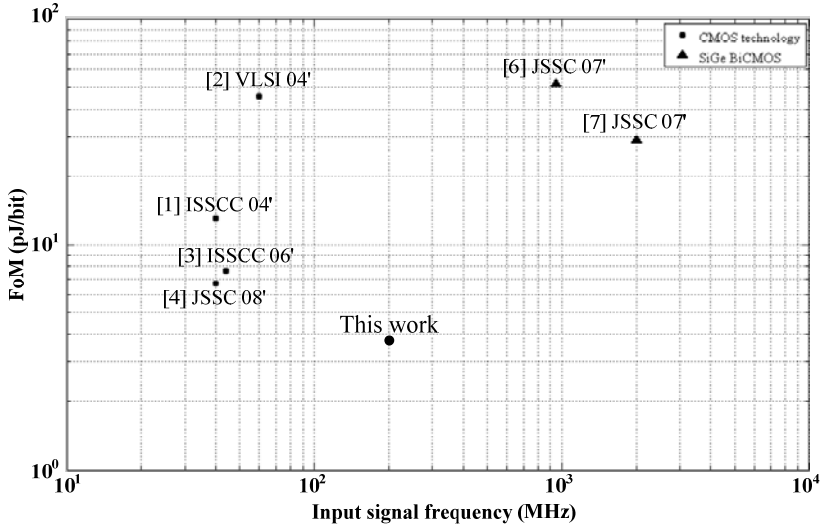
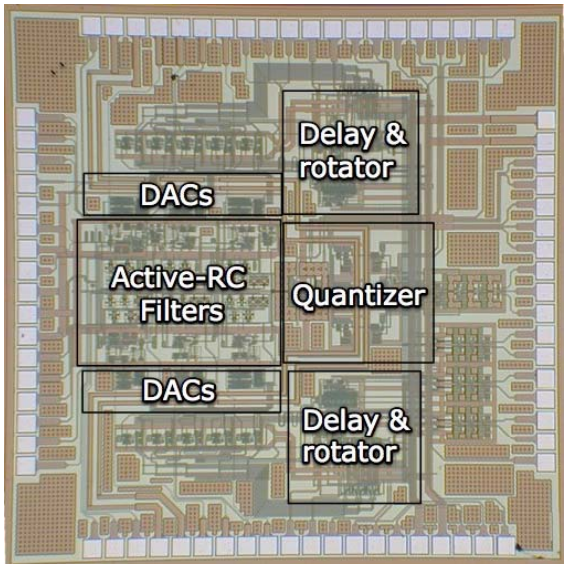


TABLE V
Comparison with Previously Reported BP ΔΣ Modulators

Reference	Technology	Fs	IF (MHz)	Band-width	Peak SNDR	IM3	Power	Area mm²	FoM (pJ/bit)
[1] BP	CMOS;0.18um	60MHz	40	2.5 MHz	69dB	-	150mW	-	13
[2] BP	CMOS;0.35um	240MHz	60	1.25 MHz	52dB	-51dB	37mW	1.2	45.5
[3] BP$^{\Delta}$	CMOS;0.18um	264MHz	44	8.5 MHz	71dB$^{\#}$	-72dB	375mW*	2.5	7.6*
[4] BP	CMOS;0.35um	60MHz	40	1MHz	63dB$^{\#}$	68dB	16mW	0.44	6.69
[6] BP	SiGe; 0.25um	3800MHz	950	1 MHz	59dB	-62dB	75mW**	1.08	51.5**
[7] BP	SiGe; 0.13um	40GHz	2000	60MHz	55dB	-	1.6W*	2.4	29*
This work	CMOS;0.18um	800MHz	200	10MHz	68.4dB	-73.5dB	160mW*	2.48	3.72*



Design Tools for Multi-Channel Filter-Bank Receiver Architectures

Sebastian Hoyos

Analog and Mixed-Signal Center
Texas A&M University

Learning Objectives

- After completing this course, you will know the fundamental design tools for modeling multi-channel filter-bank receivers.
- After completing this course, you will understand the impact of clock-jitter on time-interleaved and multi-channel filter-bank receivers.
- After completing this course, you will understand the trade-offs among power consumption, noise and area in multi-channel receivers.
- After completing this course, you will understand how to use digital background calibration to compensate non-idealities in multi-channel receivers.
- After completing this course, you will learn several applications of multi-channel receivers including multi-standard receivers .

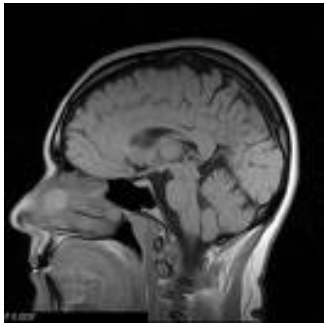
Outline

- Motivation and introduction to multi-channel receivers.
- Clock-jitter in time-interleaved ADCs and multi-channel filter-bank ADCs
- Robustness to clock-jitter in multi-channel filter-bank receivers.
- Modeling of multi-channel filter-bank receivers for design optimization.
- Digital background calibration of non-idealities in multi-channel filter-bank receivers.
- Applications

Introduction

- Ever increasing demand on Data Transmission: need larger bandwidth and dynamic range, higher data rate, etc.

MRI (magnetic resonance imaging)

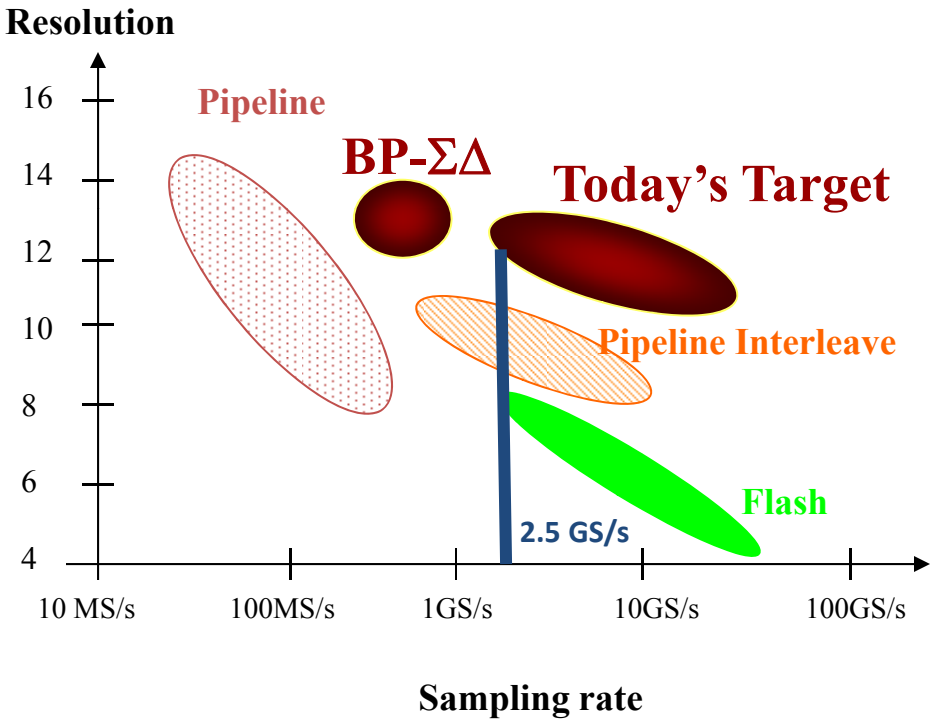


Cognitive radios

Future mmWR standards

SDR (software-defined-radio)

ADCs in nanometer CMOS technology



CMOS Nyquist ADC's: State of the art

Trends:

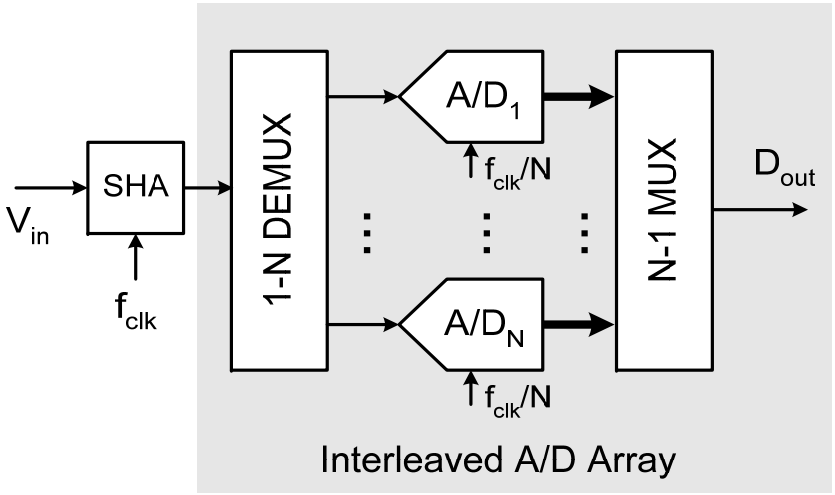
- Extensive use of parallelism
- Techniques that take advantage of digital trends
- Digital circuitry is "almost free"
- Reduced supply voltages make analog more challenging
  - **Significant PVT variations**
  - **Headroom for amplifiers**
  - **Little room for cascoding**
  - **Poor devices if V_{DS} is further reduced**

Parallel Multi-Channel ADCs

Digital intensive RF receivers -> ADCs with wide bandwidths and large dynamic range.
Solution ? -> Parallelization. Time-interleave SAR becoming very popular.

Parallelized ADCs

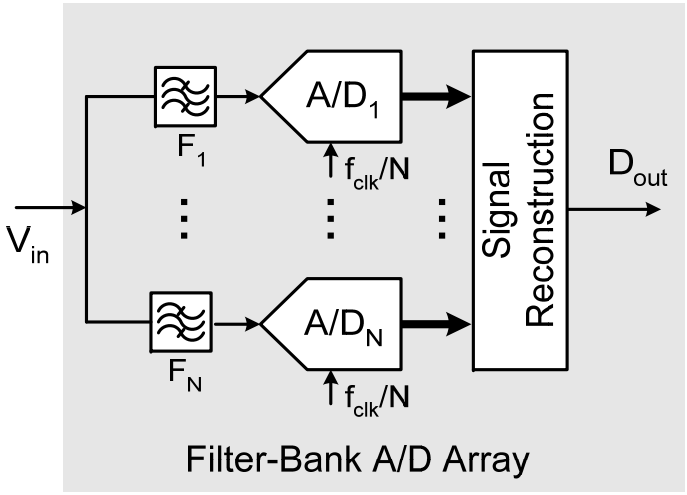
Time-interleaved ADC



Drawbacks

- SHA has stringent tracking bandwidth requirements
- Each ADC sees full input signal bandwidth (non-linearity and aliasing)

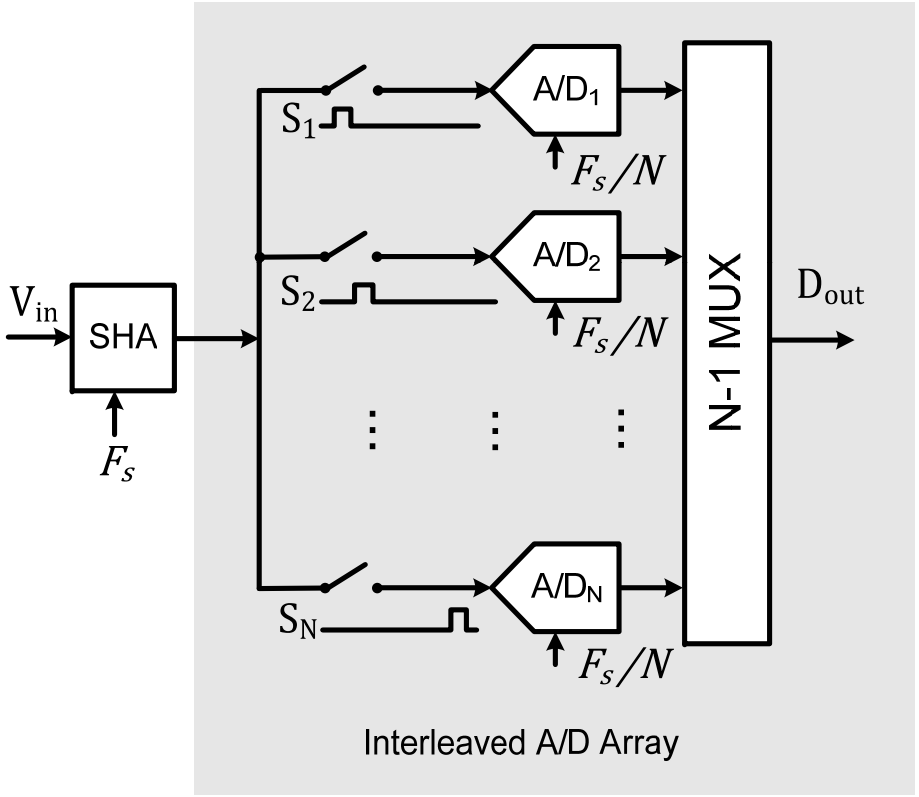
Filter-bank ADC



Drawbacks

- Filters with very tough specs (aliasing)
- Signal reconstruction increases complexity

The Clock-Jitter Limitation in Time-Interleaved ADCs



- Each ADC still sees full bandwidth of Vin ➔ suffers from aliasing of full bandwidth noise.

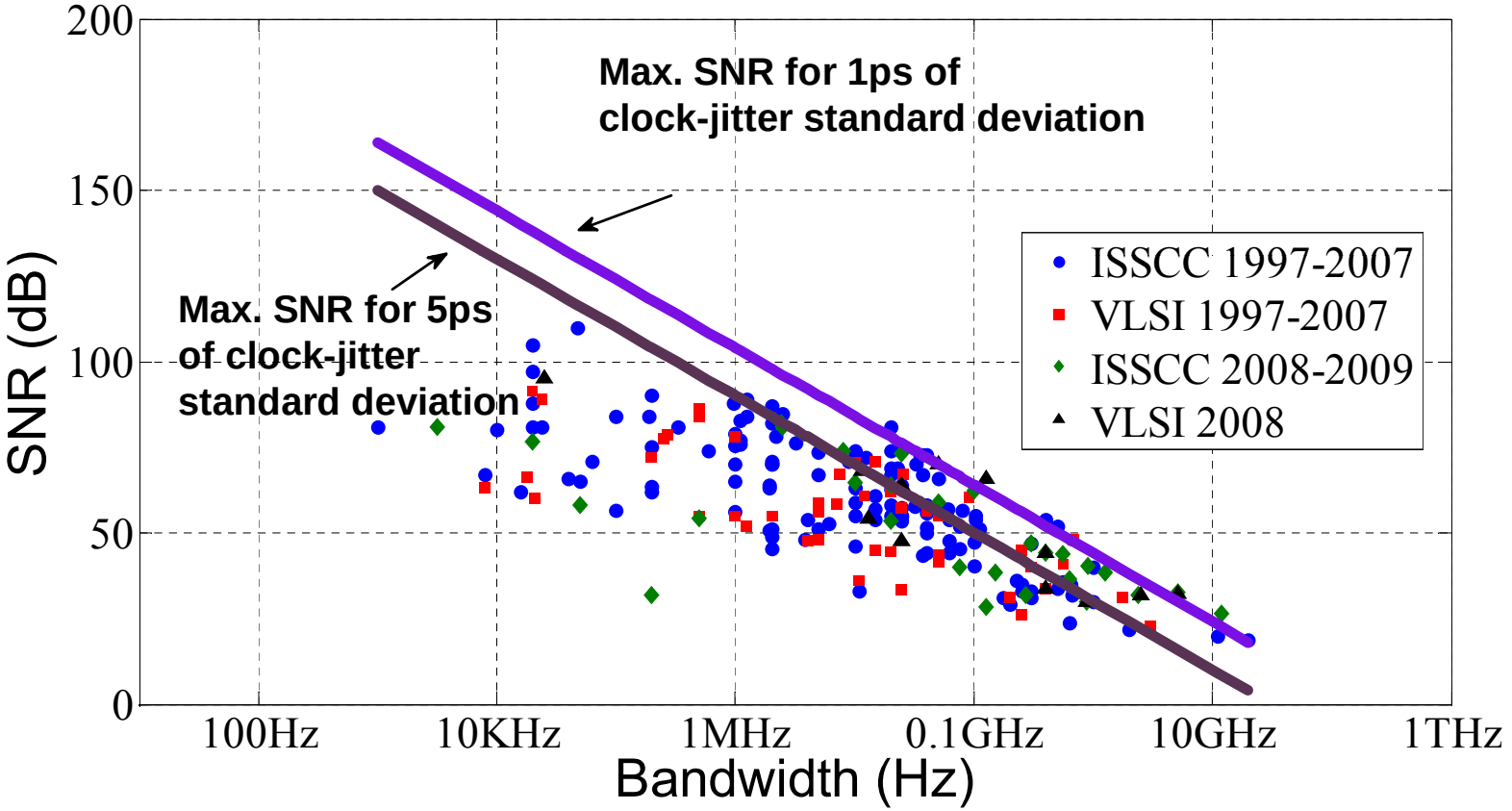
$$SNR = (1 / 2\pi \sigma_j BW)^2$$

BW	bits	SNR	σ_j
5GHz	7	44 dB	201fs
50MHz	14	84 dB	201fs

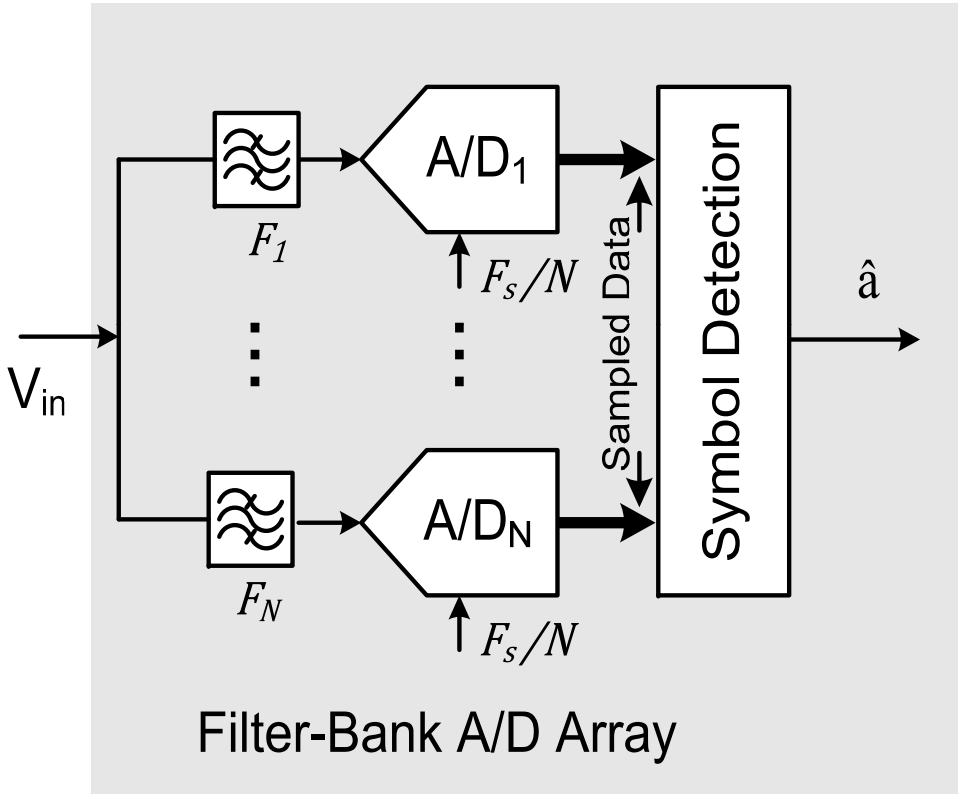
Very stringent clock-jitter specs.

- Multiple ADCs in parallel, each sampling at *Fs/N* Hz.

ADCs State-of-Art Survey



Multi-Channel Filter Bank Receiver



Basic block diagram of a multi-channel filter-bank ADC array.

- Channelization in the frequency-domain.

- Ideal reduction of noise produced by clock-jitter of variance σ_j

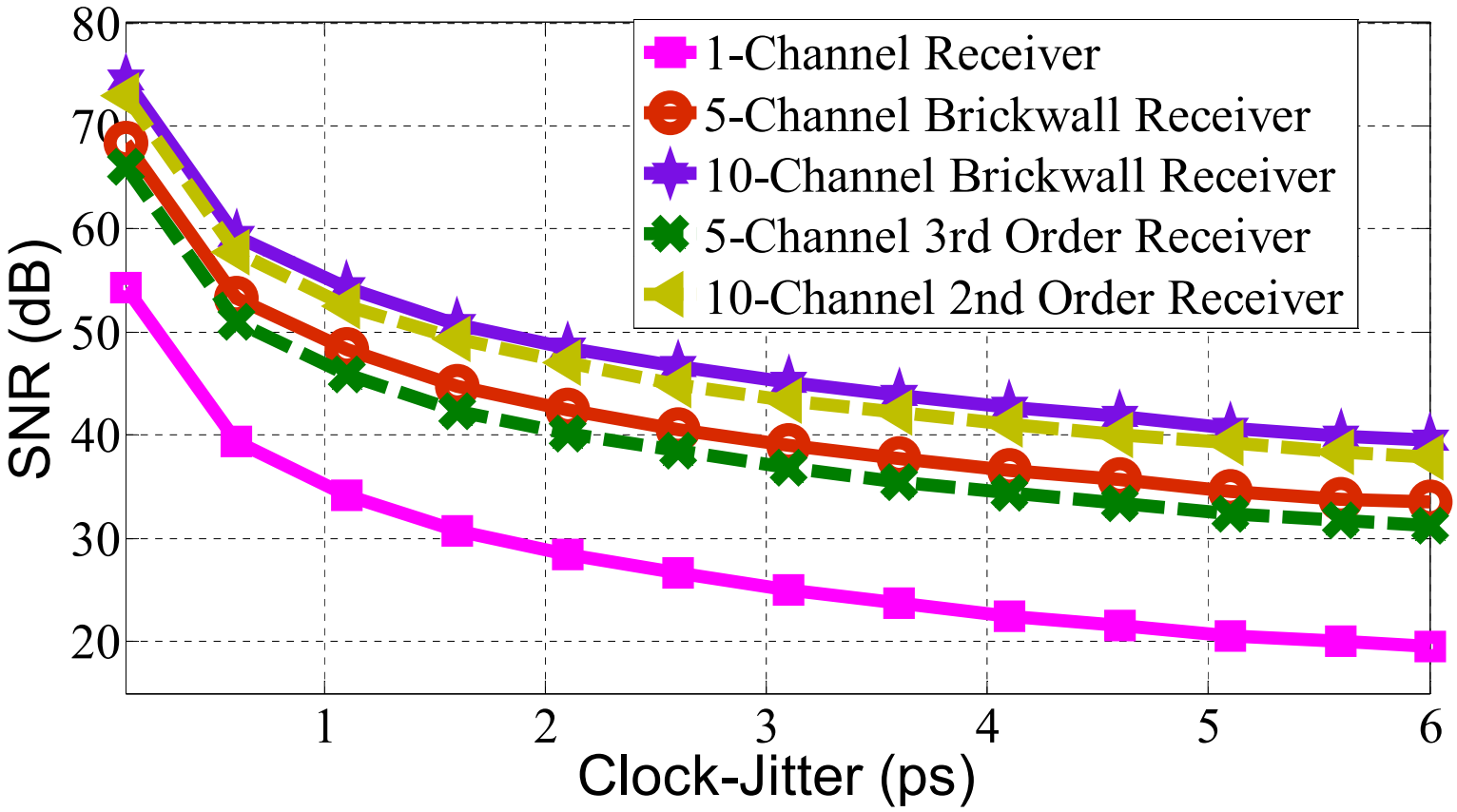
$$\sigma_n^2 = \left(\frac{2\pi\sigma_j \mathrm{BW}}{\mathrm{N}} \right)^2$$

- However, no any filter-bank can provide clock-jitter robustness.

- For instance, a first-order filter bank with filters of bandwidth *BW/N* is even worse than time-interleaving.

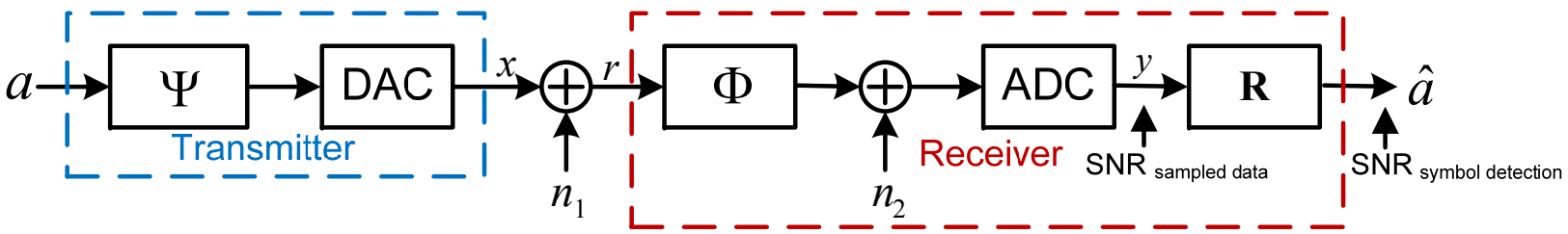
- Need optimization tools to obtain N^2 times reduction in σ_n^2

SNR vs. Clock-Jitter



- 2nd order Rx perfroms very close to brickwall Rx, 20dB enhancement.
- For 40dB SNR, 10X improvement of jitter tolerance.

Model for Receiver Analysis (1)



Block diagram that models the transmitter and multi-channel receiver including noise sources such as the clock jitter.

$$\mathrm{a} = \left[\mathrm{a}_1, \mathrm{a}_2, \ldots, \mathrm{a}_S\right]^T$$

$$\Psi = \left[\Psi_1, \Psi_2, \ldots, \Psi_S\right]$$

(Valid for any arbitrary Tx that simultaneously sends S symbols.)

n_1 : Noise added from transmission.

$x(t)$: OFDM signal composed of M sinusoidal signals.

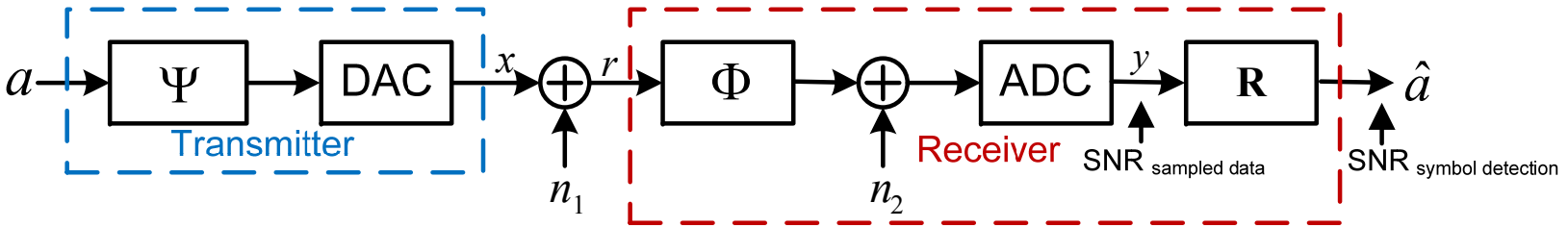
$$x(t) = \sum_{m=1}^{M} A_m \sin(m\Delta\omega t)$$

Φ : Analog filter bank transformation.

n_2 : Noise added from sampling.

$\mathbf{R}$: Symbol detection matrix.

Model for Receiver Analysis (2)



To characterize multi-channel Rx for clock-jitter tolerance, need:

- $SNR_{\text{sampled data}}$
- $SNR_{\text{symbol detection}}$

Where enhancement of SNR comes from. M is the number of tones.

$$SNR_{sampled\_data} = \frac{M}{\sigma_j^2 \Delta\omega^2 \sum_{m=1}^{M} m^2}$$

$$SNR_{symbol\_detect} = \frac{\|a\|^2}{\frac{1}{2}\sigma_j^2 \Delta\omega^2 \sum_{m=1}^{M} m^2 A_m^2 \sum_{i=1}^{S} \lambda_i}$$

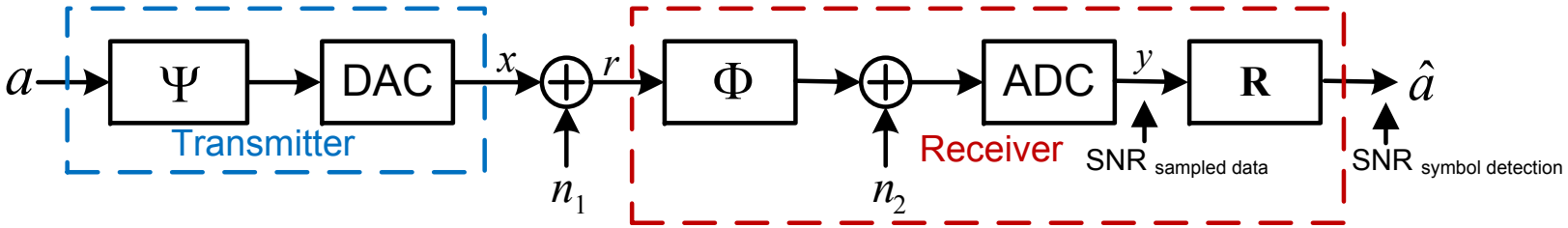
Ex: 128 tones of OFDM splits into 4 channels.

$$SNR_{Enhancement} = SNR_{M=32} - SNR_{M=128}$$

$$= 10\log\left(\frac{32}{128}\right) - 10\log\left(\frac{\sum_{m=1}^{32} m^2}{\sum_{m=1}^{128} m^2}\right)$$

≈ 12 dB

$SNR_{symbol\ detection}$ Derivation



Find noise variance, σ_n^2 first.

$$x(t)=\sum_{m=1}^{M}A_m\left[\sin(m\Delta\omega t)\cos(m\Delta\omega\delta t)\right]$$

$$\cong\sum_{m=1}^{M}A_m\sin(m\Delta\omega t)+\underbrace{\sum_{m=1}^{M}m\Delta\omega\delta tA_m\cos(m\Delta\omega t)}_{\varepsilon(t)}$$

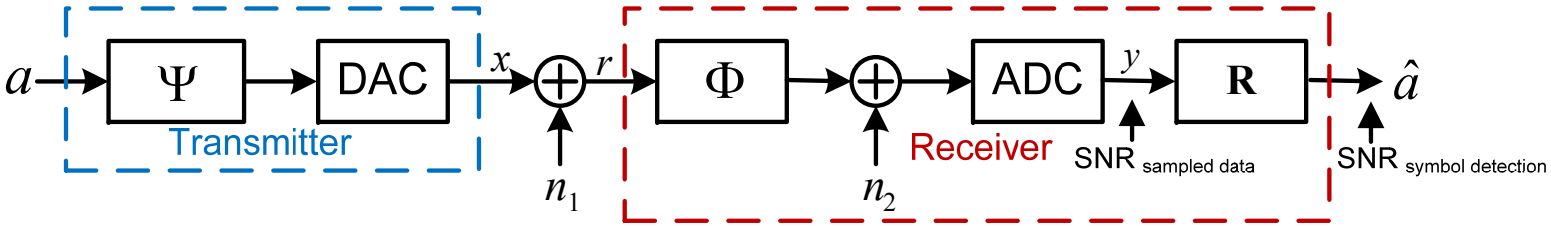
$$\sigma_n^2=\overline{\varepsilon^2(t)}$$

$$=\frac{\overline{\delta t^2}\Delta\omega}{2\pi}\int_0^{\frac{2\pi}{\Delta\omega}}\left[\sum_{m=1}^{M}m\Delta\omega A_m\cos(m\Delta\omega t)\right]^2dt$$

$$=\sigma_j^2\frac{\Delta\omega}{2\pi}\sum_{m=1}^{M}\int_0^{\frac{2\pi}{\Delta\omega}}\left[m\Delta\omega A_m\cos(m\Delta\omega t)\right]^2dt,$$

$$=\frac{1}{2}\sigma_j^2\Delta\omega^2\sum_{m=1}^{M}m^2A_m^2$$

$\mathrm{SNR}_{\text{symbol detection}}$ Derivation



$$y = \Phi(\Psi a + n_1) + n_2$$
$$= \underbrace{\Phi\Psi}_{G} a + \underbrace{\Phi n_1 + n_2}_{n}$$

$$\hat{a} = R(Ga + n) \qquad R = (G^H G)^{-1} G^H$$
$$= a + Rn$$

G: Generation Matrix

R: Symbol Detection Matrix

Now find variance of Rn

$$E\left[\|\mathbf{Rn}\|^2\right] = E\left[\mathbf{n}^H\mathbf{R}^H\mathbf{Rn}\right] = E\left[\mathbf{n}^H\mathbf{Q}^H\Lambda\mathbf{Qn}\right]$$
$$= E\left[\left(\sum_{i=1}^{S}\lambda_i n_i^*\mathbf{q}_i^H\right)\left(\sum_{j=1}^{S} n_j\mathbf{q}_j\right)\right] = E\left[\sum_{i=1}^{S}\sum_{j=1}^{S}\lambda_i n_i^* n_j\mathbf{q}_i^H\mathbf{q}_j\right]$$
$$= \sum_{i=1}^{S}\sum_{j=1}^{S}\lambda_i E(n_i^* n_j)\mathbf{q}_i^H\mathbf{q}_j = \sum_{i=1}^{S}\lambda_i E(n_i^* n_i)\mathbf{q}_i^H\mathbf{q}_i$$
$$= \sum_{i=1}^{S}\lambda_i E(\|n_i\|^2),$$

where $\mathbf{Q} = [\mathbf{q}_1^T, \mathbf{q}_2^T, \ldots, \mathbf{q}_S^T]$

$\mathbf{q}_i^T$ = eigenvector of $\mathbf{R}^H\mathbf{R}$

corresponding to the eigenvalue λ_i.

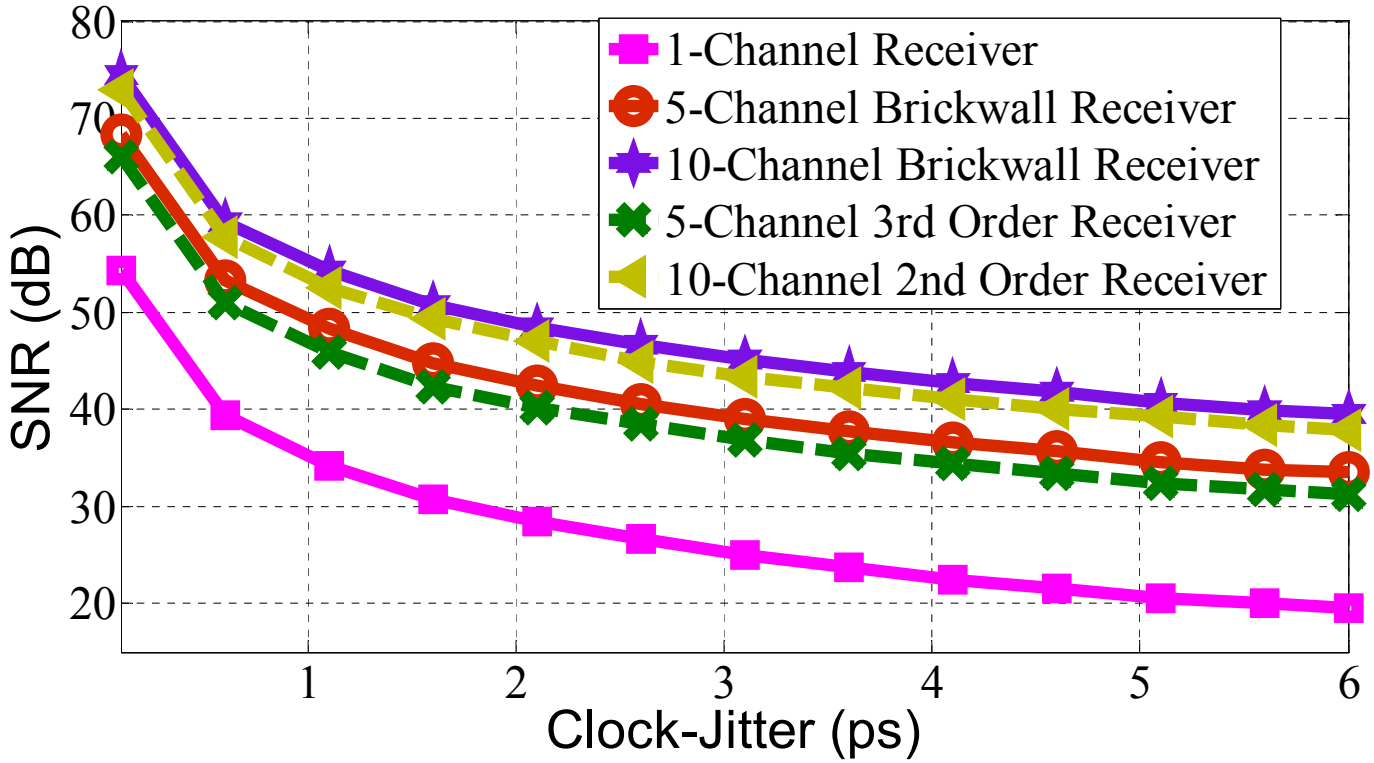
$SNR_{symbol\ detection}$ Derivation

$$E\left[\|\mathbf{Rn}\|^2\right] = \sum_{i=1}^{S} \lambda_i E\left(\|n_i\|^2\right)$$

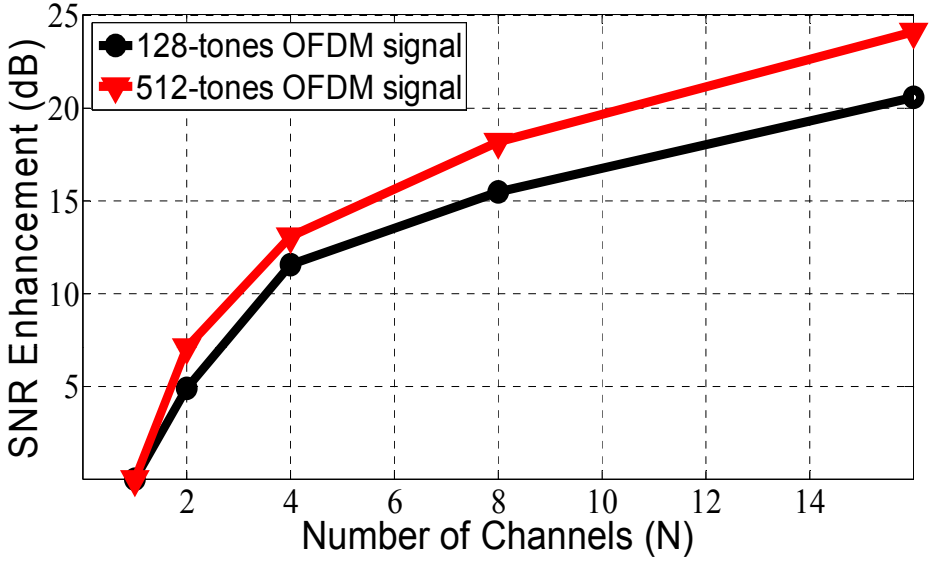
assuming noise is Gaussian, zero mean, variance = σ^2_n

$$= \sigma_n^2 \sum_{i=1}^{S} \lambda_i . \qquad \sigma_n^2 = \frac{1}{2}\sigma_j^2 \Delta\omega^2 \sum_{m=1}^{M} m^2 A_m^2$$

$$\mathrm{SNR}_{\mathrm{symbol\_detection}} = \frac{\|a\|^2}{\frac{1}{2}\sigma_j^2 \Delta\omega^2 \sum_{m=1}^{M} m^2 A_m^2 \sum_{i=1}^{S} \lambda_i}$$



Multi-Channel Receiver SNR



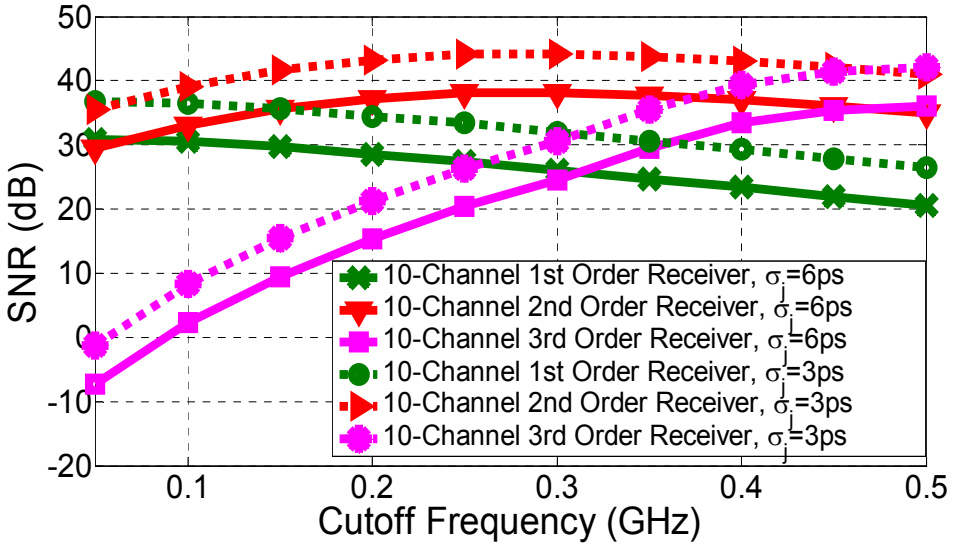
- Larger number of channel enhances SNR further.

- Signal is OFDM with BW=5 GHz.

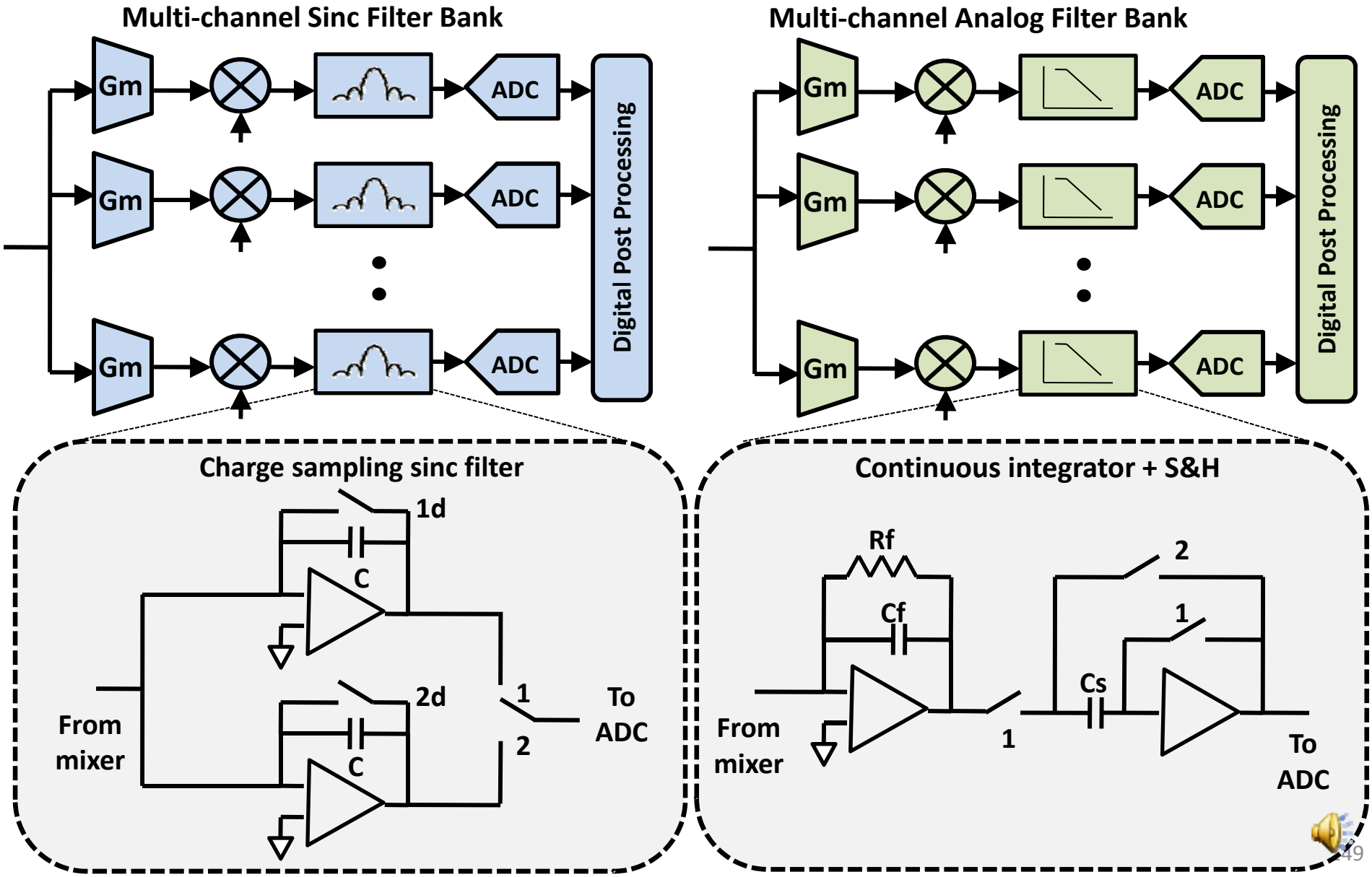
- 1st and 2nd order filters are effective in tolerating clock-jitter if BW is optimized.

- 2nd order Rx has an optimal SNR point around 300MHz.

- Reducing the BW in the 1st order filters lowers power consumption and circuit complexity.



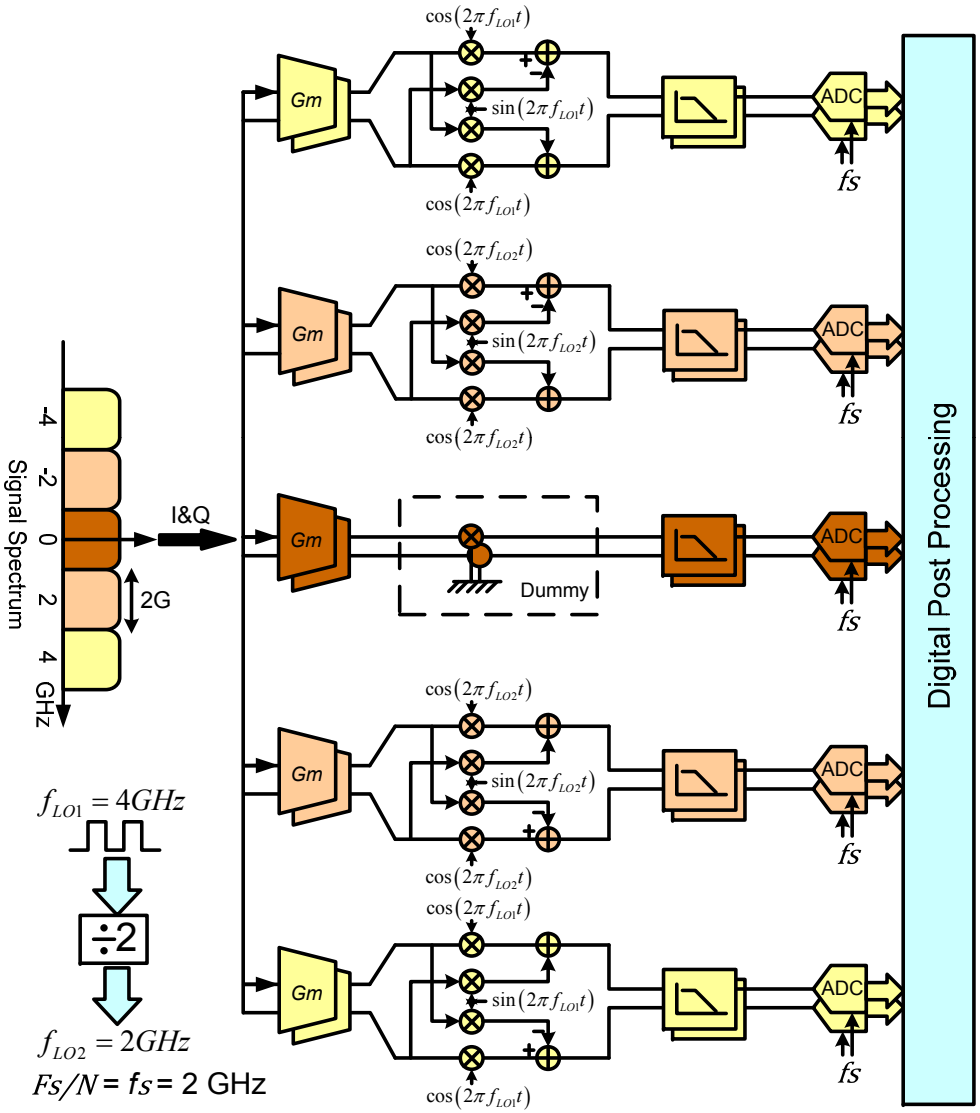
First Order Multi-Channel Filter-Bank Architecture



Analog Complexity

Sinc Filter Bank	Continuous integrator filter bank
$f_{-3dB} \approx 0.44 / Ts$	$f_{-3dB} \approx 1 / 2\pi R_f C_f$
DC gain = Gm Ts / C	DC gain = GmR_f
Int. noise = KT/C (2GmTs/C) + KT/C	Int. noise = GmR_f KT/C_f + KT/C_f + KT/C_s
GBW (op-amp 1,2) >> 1/ $2\pi R_o C$ GBW (1,2) > 7/(settling time) (β~1) (10bits)	GBW (1) >> 1/ $2\pi R_f C_f$ GBW (2) > 7/(settling time) (β~1) (10bits)
Example: Assuming Gm = 1mA/V, Ts = 4ns,	
DC gain = 4, $f_{-3dB} \approx$ 110MHz	For DC gain = 4, Rf = 4K For $f_{-3dB} \approx$ 110MHz, $C_f \approx C/3$
Noise = 9KT/C	Noise = 13KT/C + KT/C_s
GBW (1,2) ≈ 1.75 GHz	GBW (1) ≈ 1.5 GHz (as $C_f \approx C/3$) GBW (2) ≈ 3.5 GHz (for settling time = 2ns)

Rx Block Diagram with I&Q Mixing

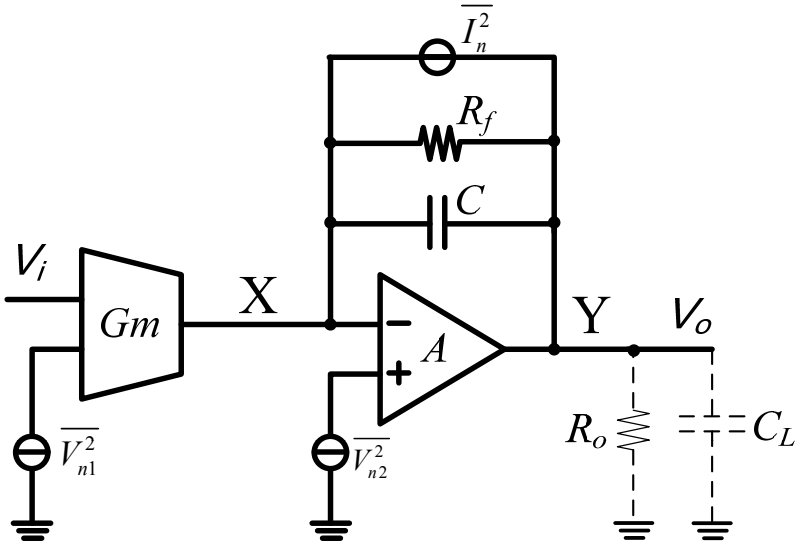


- Block diagram of proposed multi-channel receiver with I&Q 10 GS/s and SNR=40 dB (10 channels, of which only 5 are shown in Fig.). All the clocks can tolerate up to 5 ps of clock-jitter standard deviation.

- Now, realization of MRI, cognitive radio, SDR, and other wideband communication systems become feasible.

- Low complexity in clock generation; critical power savings (lower frequency.)

Noise, Power, and Area Trade-offs



Block diagram of a first order filter based on a continuous-time integrator.

$$V_{n,sampled}^2 = \frac{kT}{C}\left(GmR_f + 1\right) + \frac{kT}{C_L}$$

- Much more technology scalable than conventional time interleaved ADCs.

- N filters of bandwith BW/N each consumes the same or lower power comparing with one filter with bandwidth of BW.

- G_m needs to be reduced to lower BW. ➔I_{bias} and W can be sized (2 degrees of freedom.)

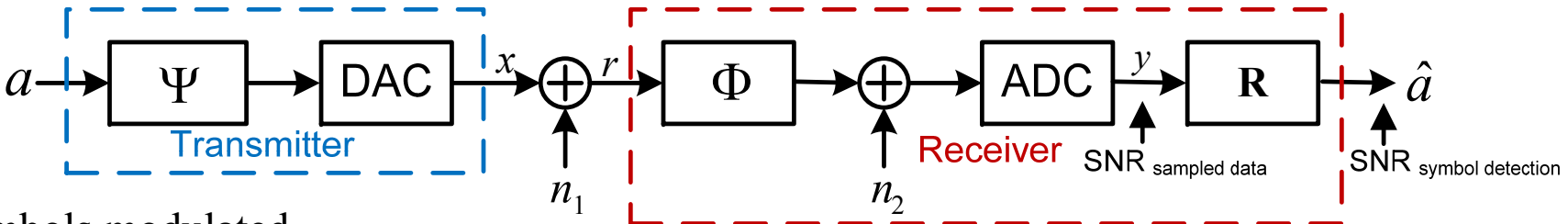
$$G_m = \sqrt{\frac{KI_{bias}W}{L}}$$

Gain	G_mR_f
BW	$\frac{1}{R_fC}$
Power	$\propto G_m$
Noise	$\frac{\eta kT}{C}$

Multi-Channel Receiver Non-idealities

- Gain and Phase Mismatches between different paths.
- Phase offsets in the Carriers
- Frequency offset in the Carrier Frequencies
- Frequency offset in the Mixing LO's

Least Squares Data Estimation



Input symbols modulated on carriers $\vec{a} = [a_i(0), a_q(0), a_i(1), a_q(1), \ldots a_i(K), a_q(K)]$

Output sampled basis coefficients $\vec{y} = [Y_{0,0}, Y_{0,1}, \ldots Y_{0,N-1}, Y_{1,0}, Y_{1,1}, \ldots Y_{M-1,N-1}]^T$

Entire system represented as a linear transformation from data symbols (a) to output samples of multi-path receiver (y)

$$G\vec{a} = \vec{y} \quad \text{, where} \quad G=\Psi\Phi$$

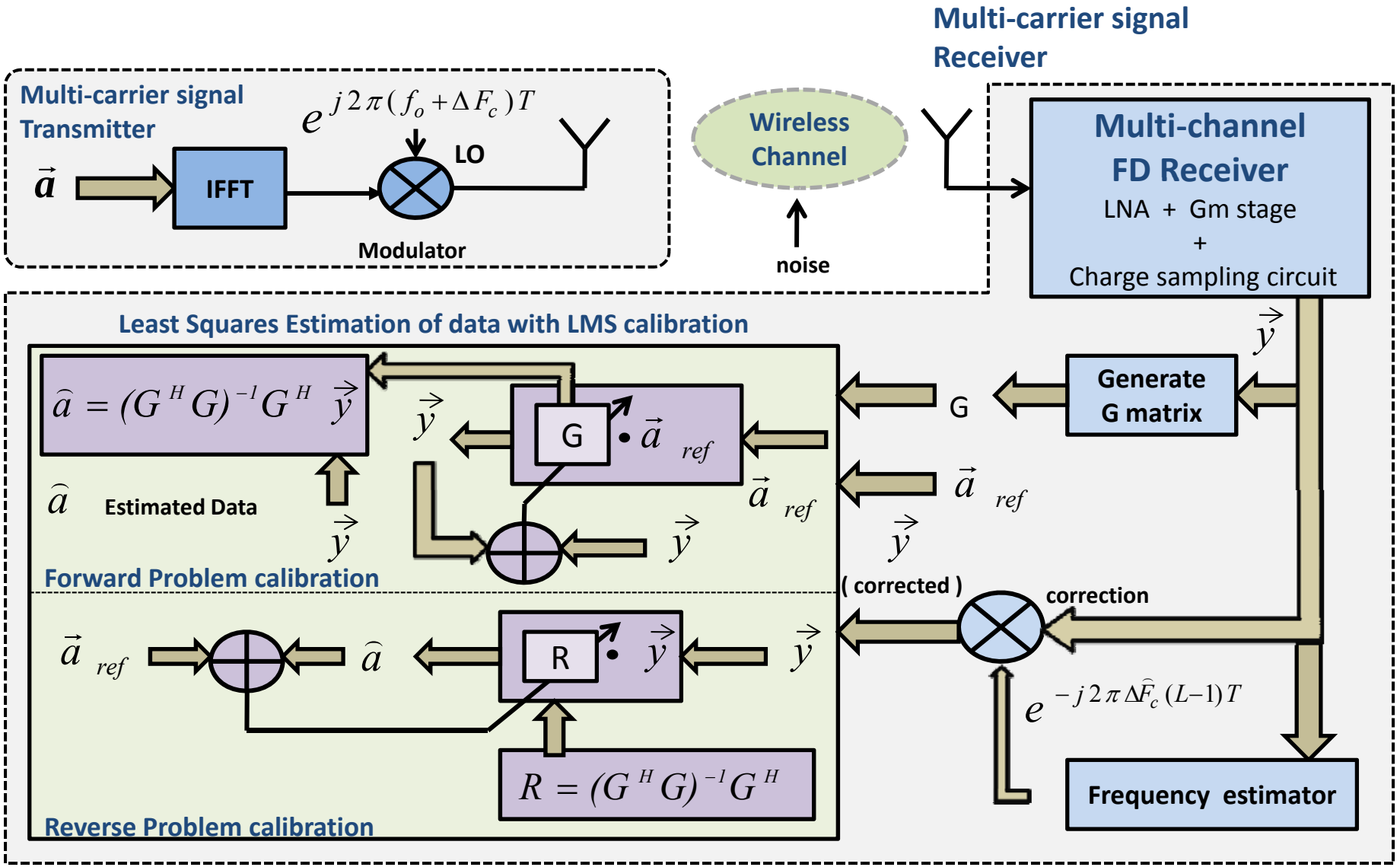
Least Squares (LS) solution for the system -> $R=(G^H G)^{-1} G^H$

Estimate Equation -> $R\vec{y} = \vec{a}$

Where *G and R* are the Generation Matrix and Symbol detection matrix respectively.

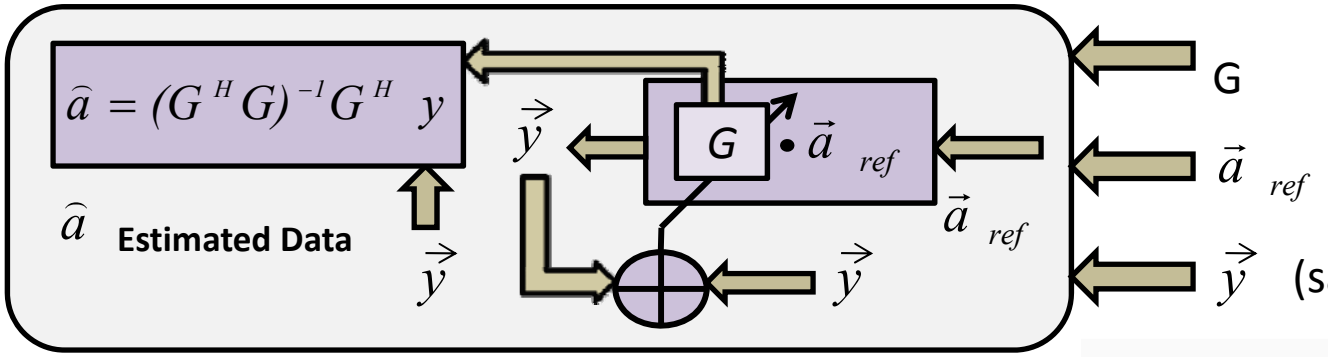
R is sensitive to mismatches, imperfections and offsets in the system, therefore it has to be calibrated to give good SNDR. Least Mean Squares(LMS) has been adopted for calibration of *R*. Note that the frequency offset causes a time varying error to be introduced therefore it has to be estimated and corrected before the actual calibration of *R*.

Complete System Calibration



Digital Background Calibration based on LMS

Forward Problem Calibration



(samples from receiver)

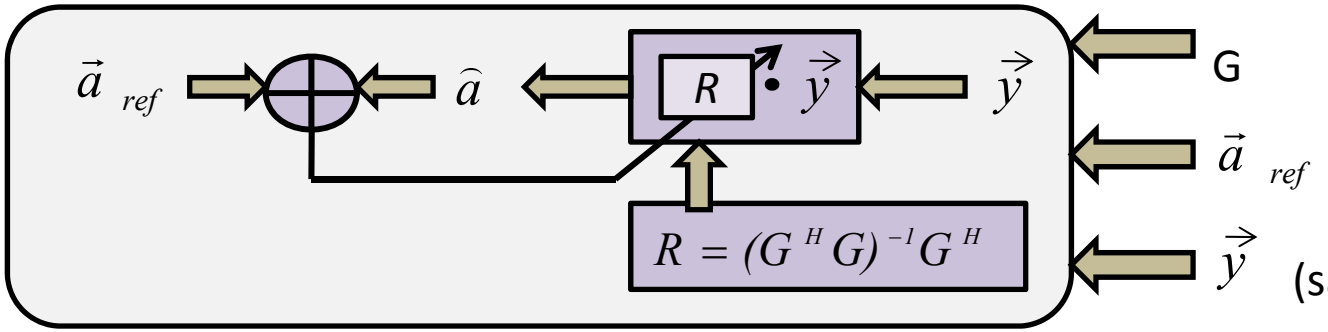
Forward Problem equation

$$G\vec{a} = \vec{y}$$

Forward Problem update equation

$$\hat{G}(L+1) = \hat{G}(L) + \frac{\vec{e_y}(L) * \vec{a}}{\|a\|^2}$$

Reverse Problem Calibration



(samples from receiver)

Reverse Problem equation

$$\vec{a} = R\vec{y}$$

Reverse Problem update equation

$$\hat{R}(L+1) = \hat{R}(L) + \frac{\vec{e_a}(L) * \vec{y}}{\|y\|^2}$$

Digital Background Calibration based on LMS

Initialization of G matrix

Input -> a1 a2 a3 . . . . aS

Output -> r1 r2 r3 . . . . rS

a1 -> [1 0 0 0 . . . 0] ^{T}
a2 -> [0 1 0 0 . . . 0] ^{T}
a3 -> [0 0 1 0 . . . 0] ^{T}

r1 forms 1st column of G matrix
r2 forms 2nd column of G matrix
r3 forms 3rd column of G matrix

aS -> [0 0 0 0 . . . 1] ^{T}

rS forms Sth column of G matrix

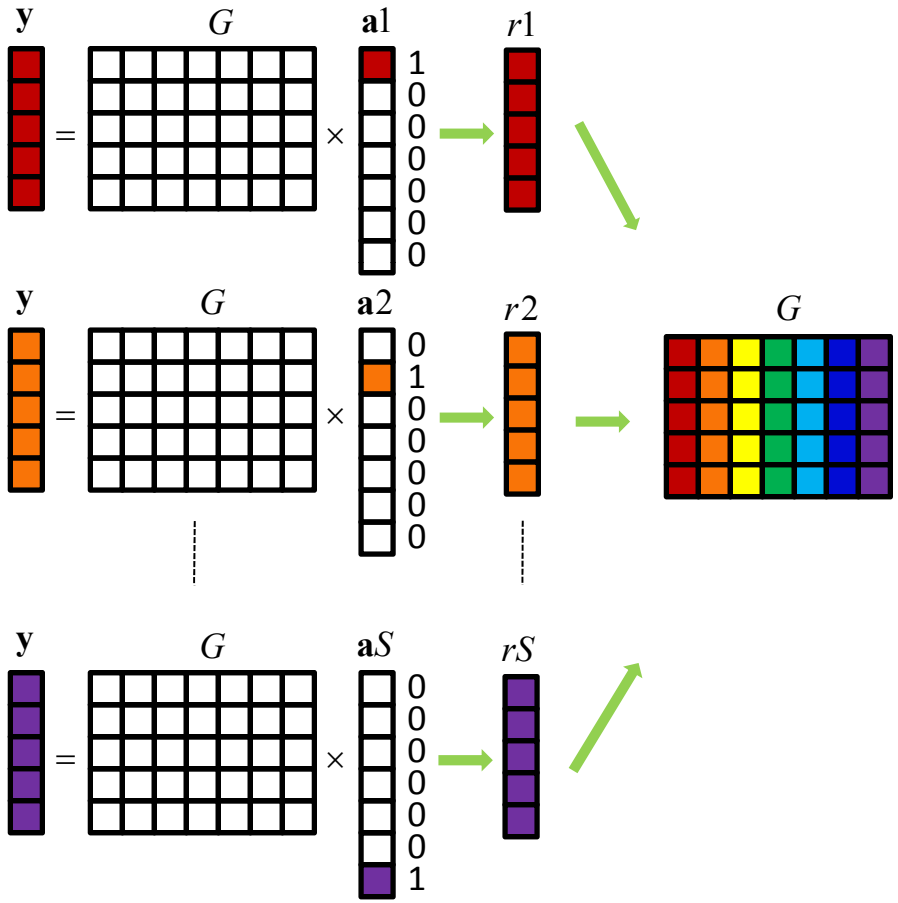
Once the frequency offset has been estimated, we form the Generation matrix by scanning the carriers. The above data pattern is sent to scan the carriers. Once this formation is done, calibration of the formed matrix starts.

LMS calibration

Two methods:

1. **Forward Problem Calibration**
2. **Reverse Problem Calibration**

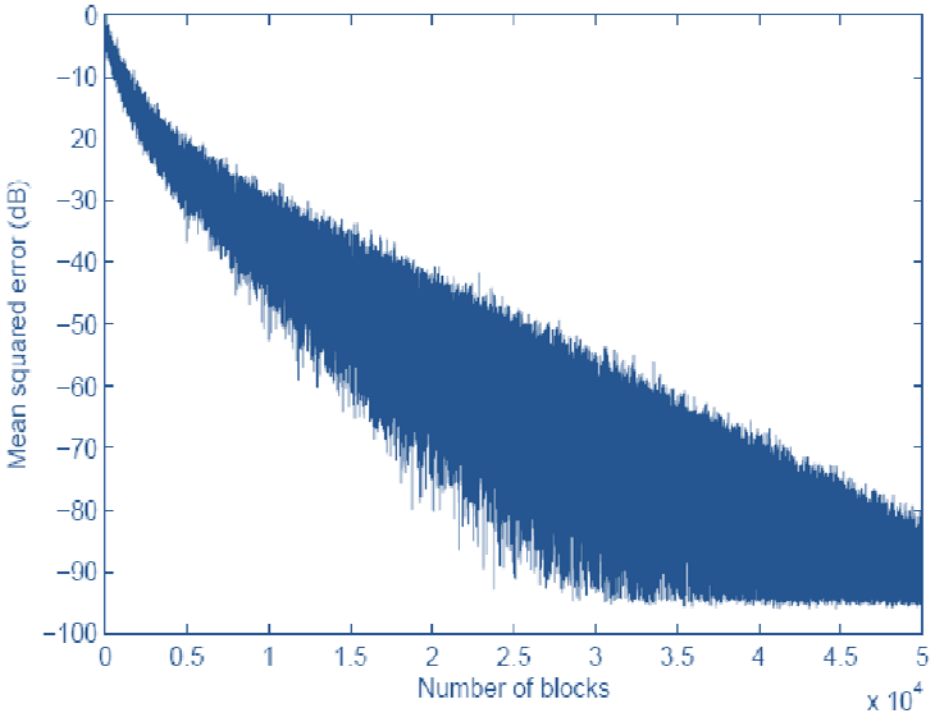
Initialization of G matrix (Graphical Explanation)



Simulations

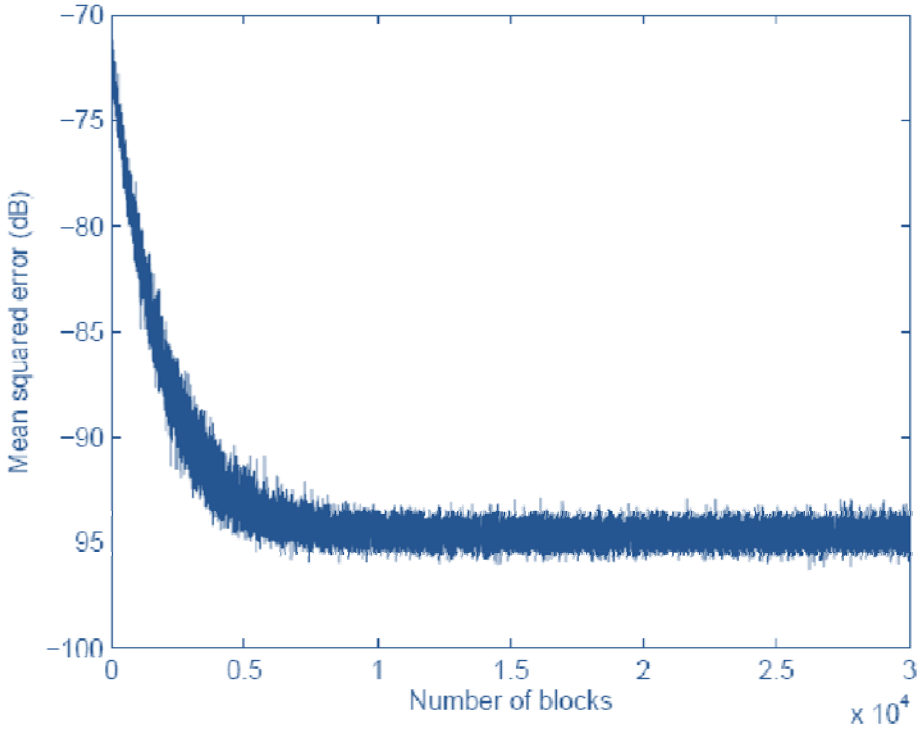
Mean squared error convergence

1. With arbitrary R matrix



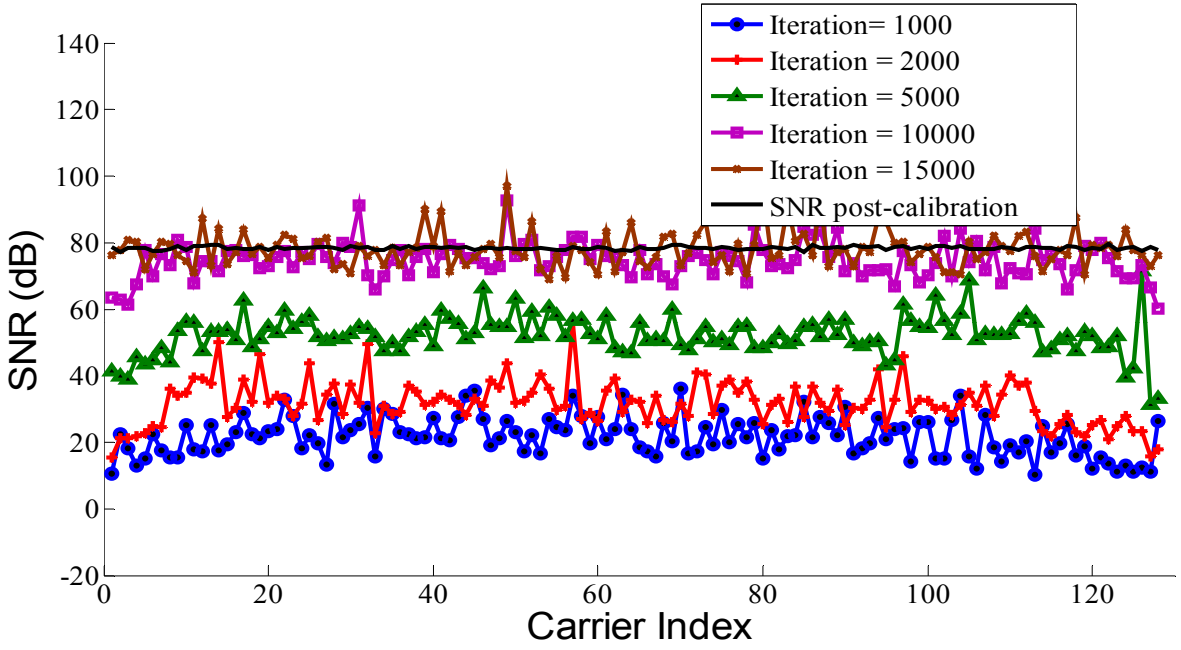
Very slow convergence

2. With R matrix initialized from ‘y’ vector



Fast convergence

SNR vs. Iterations



-All multi-channel systems are sensitive to mismatches in key blocks.

-Digital back-end detects the symbols from ADC output, and has the LMS algorithm learning the mismatches in Rx.

-Controlled mismatches are between different channels.
Gain variation: 10~20%
Phase mismatch: 10~15%
Mismatch in the type of LO signal added.

Calibration algorithm improves the Rx SNR from 20dB to 80dB.

Digital Complexity

Sparsity of $(G^HG)^{-1}$

G^HG is denoted by $X = [X_{i,j}]_{S\times S}$

$$X_{i,j} = \sum_{m=0}^{M-1}\sum_{n=0}^{N-1} e^{-j2\pi(i-j)m/M} Q_{i,n}Q^*_{j,n}$$

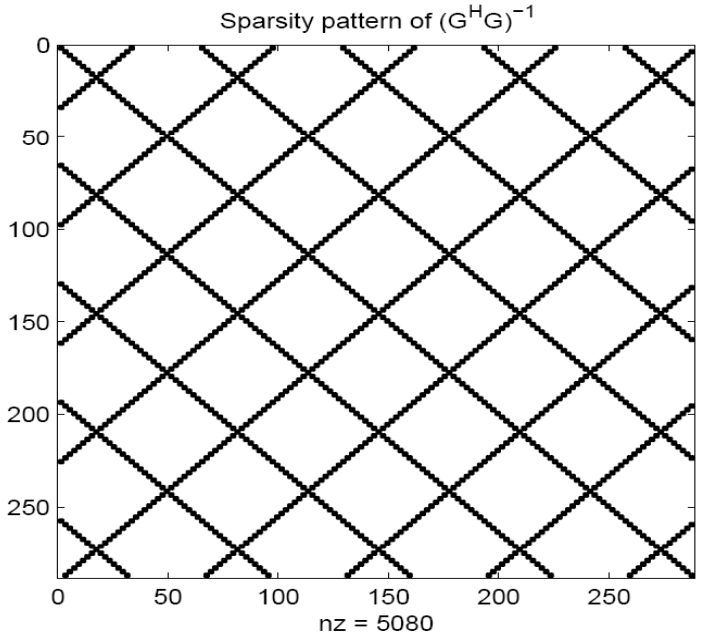
$$= \sum_{n=0}^{N-1} Q_{i,n}Q^*_{j,n} \sum_{m=0}^{M-1} e^{-j2\pi(i-j)m/M}$$

$$X_{i,j} = \left\{ \begin{array}{ll} M\sum_{n=0}^{N-1} Q_{i,n}Q^*_{j,n} & (i-j) mod\, M = 0 \\ 0 & otherwise \end{array} \right\}$$

$X_{i,j}$ is non-zero only when (i-j) mod M = 0

- G^HG has only 2N non-zero elements in each row
- Inverse of G^HG also has the same sparsity.

  Complexity of computation of
  - **G^HG -> o(2N x 2N x 2S) = o($8N^2S$)**
  - **$(G^HG)^{-1}$ -> o(2N x 2N x 2S) = o($8N^2S$)**



Digital Complexity

Step 1: $\vec{p} = G^H \vec{y}$ Complexity: o(4S(logM + N))

Step 2: $\hat{a} = (G^H G)^{-1} \vec{p}$ Complexity: o(4NS)

Total Complexity of LS estimation : o(4S(logM + N)) + o(4NS)

Example: S = 128, M = 32, N = 5

Complexity of FFT: o(4SlogS) = **o(28S)**

Complexity of LS estimate,

Sinc filter bank: o(4S(logM + N)) + o(4NS) = **o(60S)**

Analog filter bank: o(4NMS) = **o(640S)**

Complexity of estimation during LMS calibration

Forward Problem:

$$a = R\vec{y}$$
$$= \underbrace{(G^H G)^{-1}}_{o(16N^2S)} \underbrace{G^H y}_{o(4S\ (logM+N))}$$

o(4NS)

Reverse Problem:

$$a = \underbrace{R\vec{y}}_{o(4NMS)}$$

Example: S = 128, M = 32, N = 5

Forward Problem:

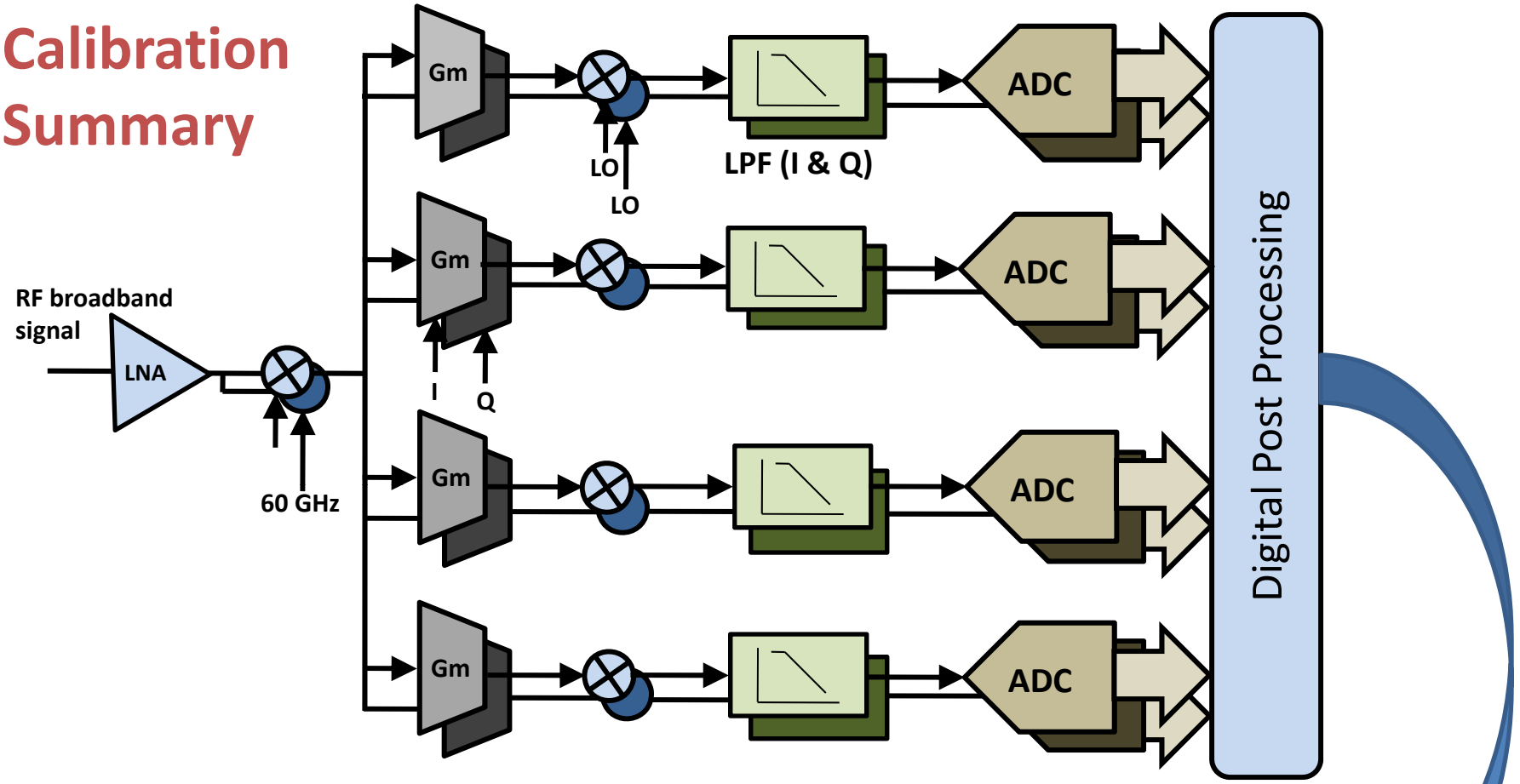
o(16N²S) + o(4S (logM+N)) + o(4NS) = **o(460S)**

Reverse Problem:

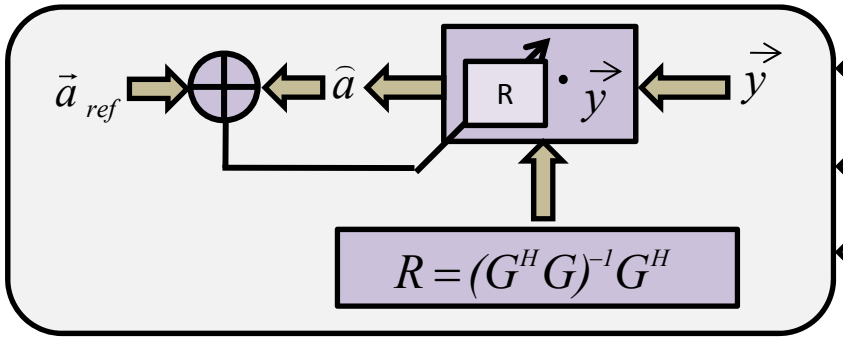
o(4NMS) = **o(640S)**

Comparative Study	Sinc Filter Bank	Analog Filter Bank
Analog Front end complexity	Larger capacitors No resistor required. Reset ensures finite DC gain. Lesser noise Smaller GBW for op-amps.	Smaller capacitors Resistor required for finite DC gain. Noise is high. Larger GBW for op-amps.
Analog Power consumption	Less	4 times higher
Digital complexity (Estimation)	o (4S (N + logM)) + o(4NS) Example: o (60S)	o (4NMS) Example: o (640S)
Digital complexity (Estimation @ calibration)	$o(16N^2S)$ + o(4S (logM+N)) + o(4NS) Example: o(460S)	o (4NMS) Example: o (640S)
Digital power consumption	Low Example: About 10% of power of analog filter	High Example: 10 times more power than sinc filter

Calibration Summary



Reverse Problem Calibration



G

$\vec{a}_{ref}$

$\vec{y}$ (samples from receiver)

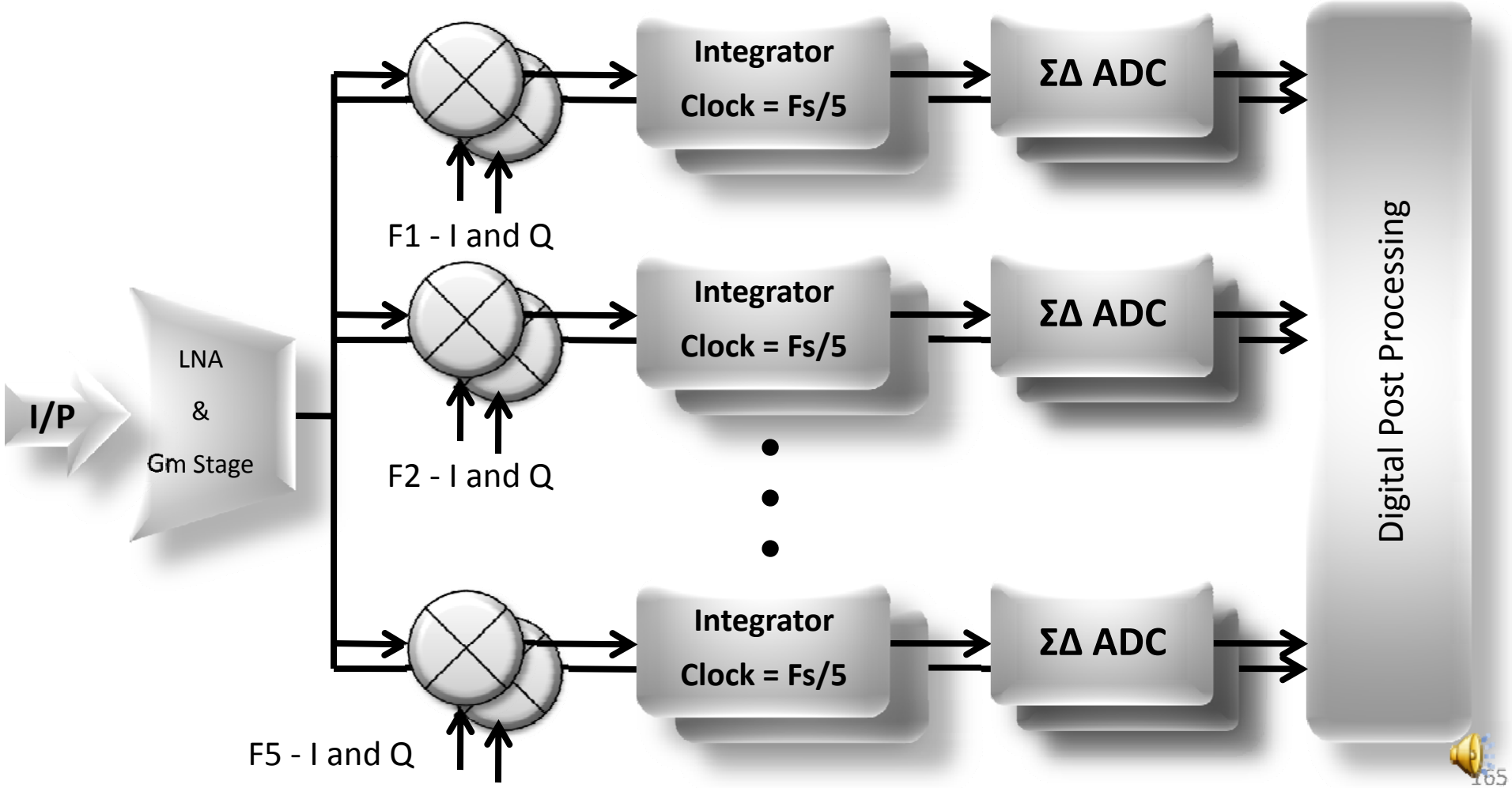
Reverse Problem equation

$$\vec{a} = R\vec{y}$$

Reverse Problem update equation

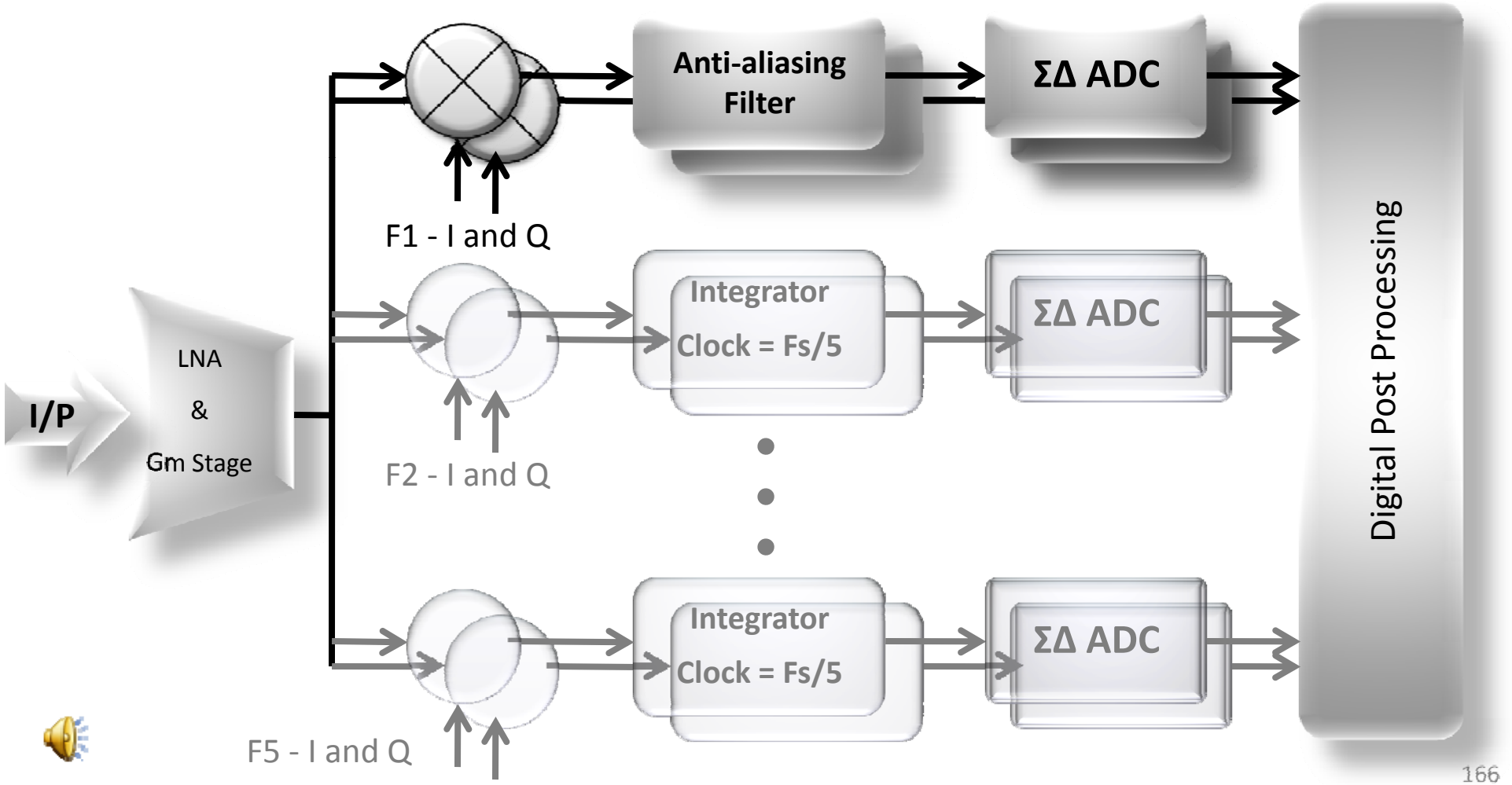
Multi-Standard Receiver Front-end

STANDARD	SPECIFICATIONS
UWB	500 M S/s and 5 bits
802.11 G	50 M S/s and 8 bits
Bluetooth	1 MHz and 12 bits
GSM	200 KHz and 14 bits



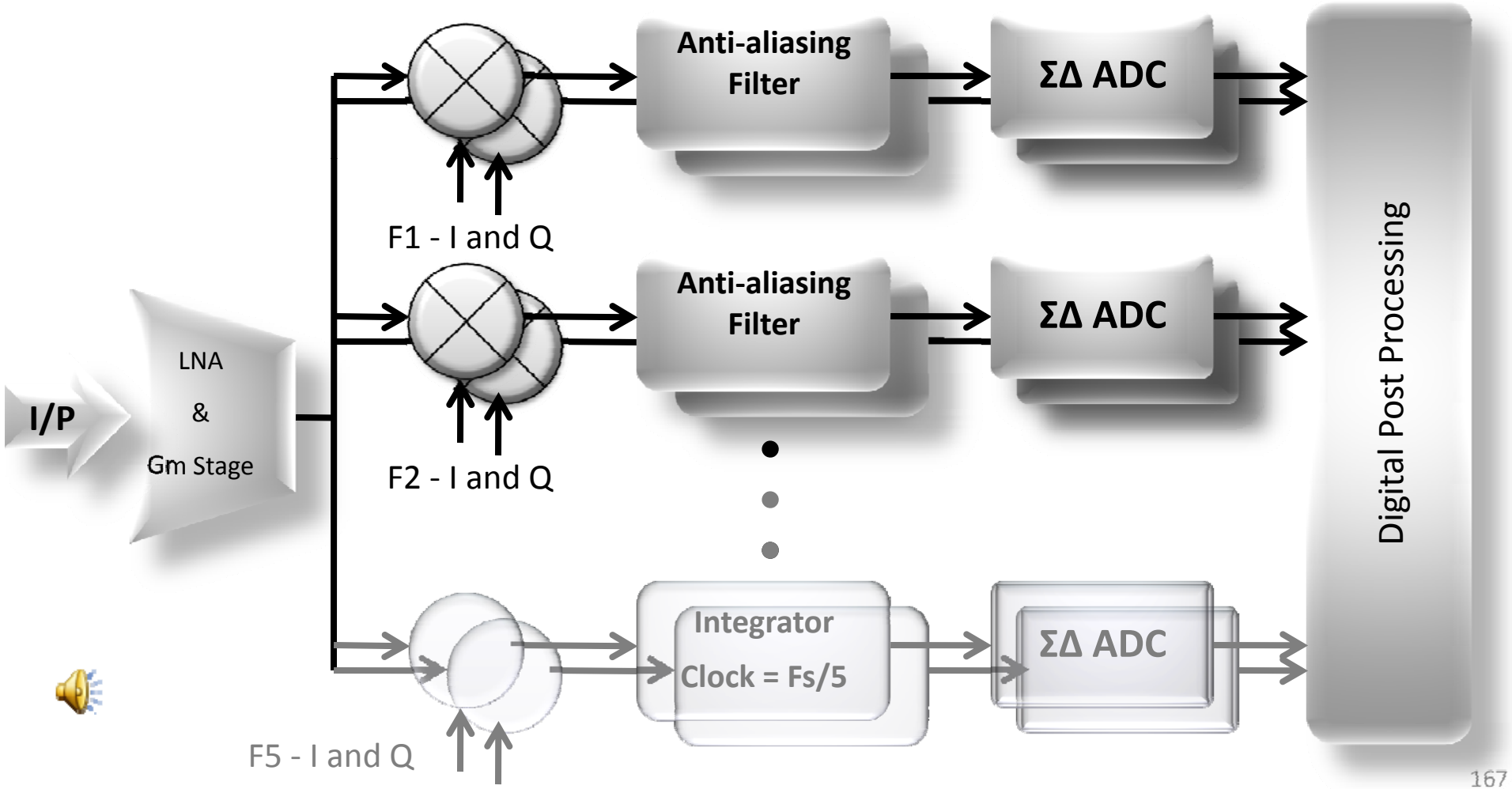
Multi-Standard Receiver Front-end

GSM	200 KHz and 14 bits
Bluetooth	1 MHz and 12 bits



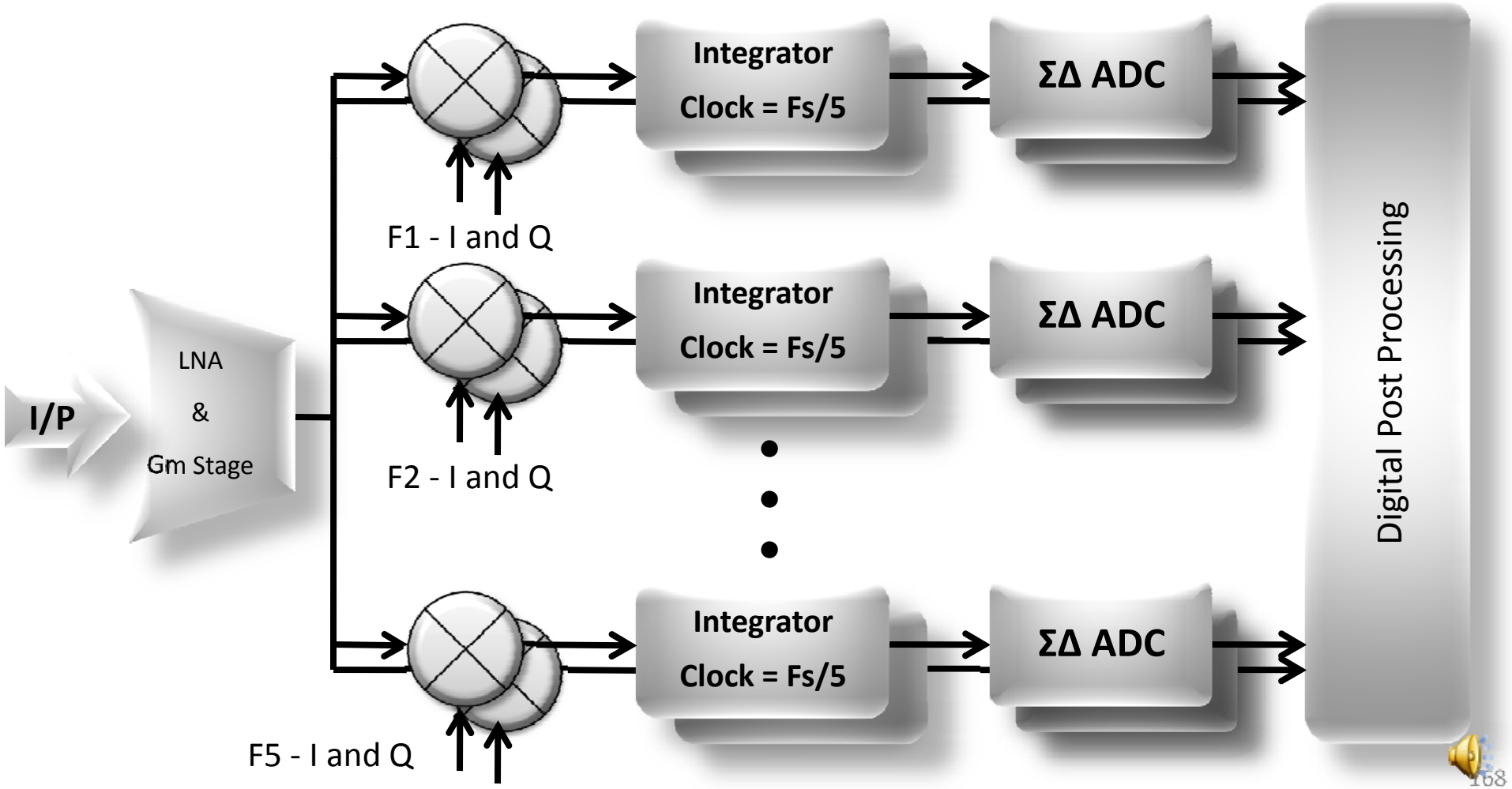
Multi-Standard Receiver Front-end

802.11 G	50 M S/s and 8 bits

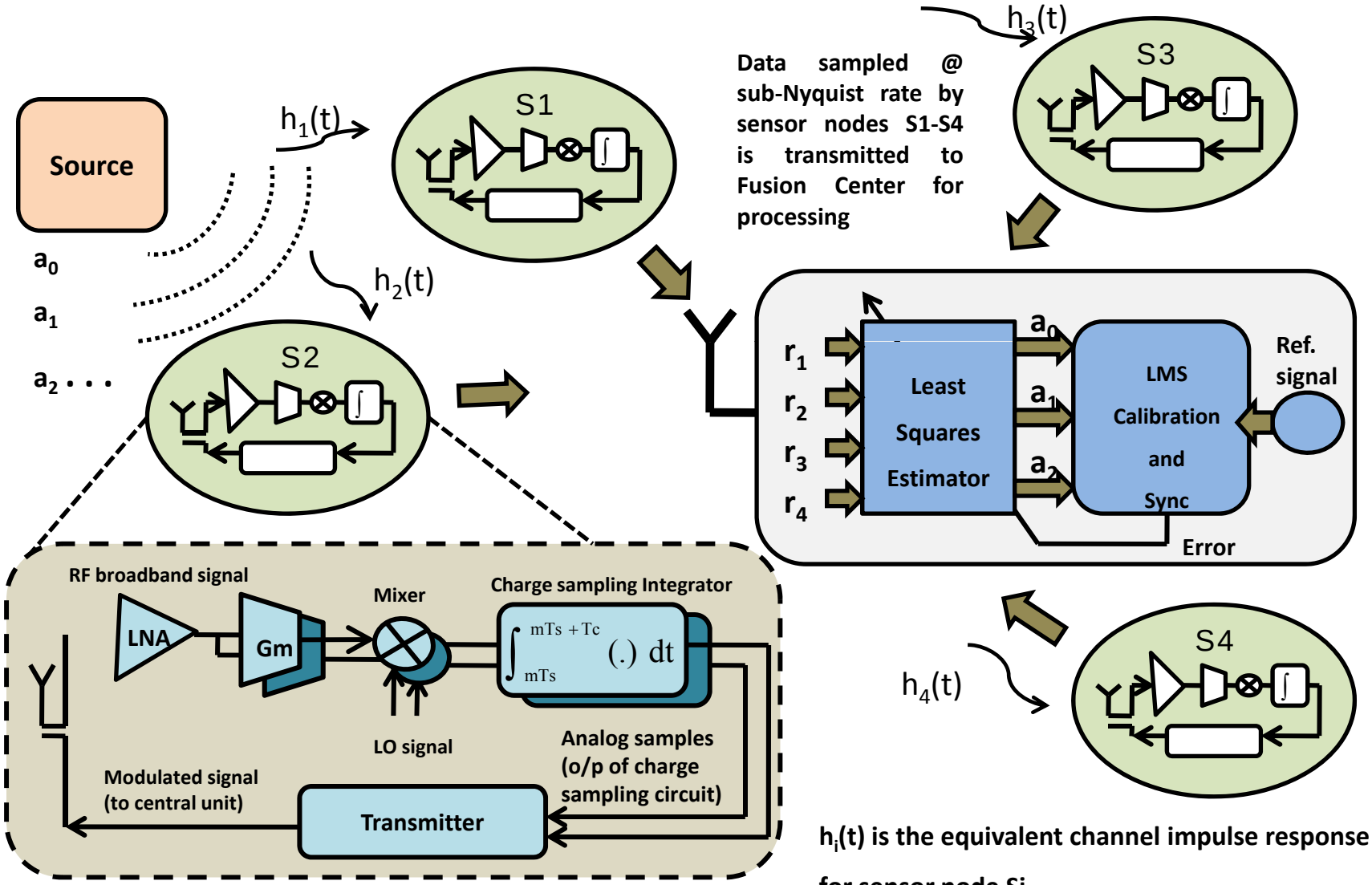


Multi-Standard Receiver Front-end

UWB	500 M S/s and 5 bits



Decentralized Sensor Network



$h_i(t)$ is the equivalent channel impulse response for sensor node Si

Summary and Conclusions

- Optimal design of baseband multi-channel receivers with robustness to clock-jitter will open a large number of possibilities in future wideband communication applications.

- Design example of 5GHz baseband signal with 40dB of SNR with sampling clock that can tolerate 5ps (standard deviation) is introduced.

- Very low complexity multi-channel digital background calibration techniques can compensate the nonidealities.

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10. "2009 international microwave symposium at the radio-frequency integrated circuit workshop titled: Challenges for future RF integration," http://www.ims2009.org/workshop_descrip.htm#WSG.

Post-test Questions

1. In a time-interleaved ADC topology with Nyquist sampling rate of 10 GS/s, what is the rms clock-jitter requirement for a SNR=44 dB if a single tone input is used?
   a) 201 ps_{rms} (correct)
   b) 500 ps_{rms}
   c) 1 ps_{rms}
   d) 5 ps_{rms}

   The correct answer is “a)”, which can be obtained from the SNR equation discussed in slide 7.

2. In a time-interleaved ADC topology with Nyquist sampling rate of 10 GS/s, what is the rms clock-jitter requirement for a SNR=40 dB if a 128-tone input is used?
   a) 201 ps_{rms}
   b) 500 ps_{rms} (correct)
   c) 1 ps_{rms}
   d) 5 ps_{rms}

   The correct answer is “b)” which can be obtained directly from the figure in slide 10. Note that multi-tone signals have lower jitter specifications.

Post-test Questions

3. In a 10-channel brickwall multi-channel filter-bank receiver topology with sampling rate of 20 GS/s, what is the rms clock-jitter requirement for a SNR=40 dB if a single tone input is used?
   a) 201 ps_{rms}
   b) 500 ps_{rms}
   c) 2 ps_{rms} (correct)
   d) 5 ps_{rms}

   The correct answer is "c)" which can be derived from the equation in slide 10. Note also that the jitter requirement is 10 times smaller than in time interleaved ADCs.

4, In a multi-channel filter-bank receiver topology with sampling rate of 20 GS/s, what is the rms clock-jitter requirement for a SNR=40 dB if a 128-tone input is used?
   a) 201 ps_{rms}
   b) 500 ps_{rms}
   c) 1 ps_{rms}
   d) 5 ps_{rms} (correct)

   The correct answer is "d)" which can be obtained from the figure in slide 10.

Post-test Questions

5. Due to the sparsity of the detection matrix in sinc filter banks, how many times is the digital detection complexity reduced?
   a) 2 times
   b) 5 times
   c) 7 times
   d) 10 times (correct)

   The correct answer is “d)” which was derived in slide 30.

6, How much is the gain-bandwidth product reduction of a sinc filter versus a continuous-time filter for a 10-bit settling error?
   a) 2 times (correct)
   b) 5 times
   c) 7 times
   d) 10 times

   The correct answer is “a)” which was summarized in slide 18 but the derivation was not provided but left as homework to the reader..

Post-test Questions

7. When comparing the silicon area of a multi-channel receiver versus a single-channel receiver, we can say that:
   a) They are the same
   b) Multi-channel has an area overhead (correct)
   c) Multi-channel occupies less area

   The correct answer is “b)” which was discussed in slide 20.

8. When comparing noise performance and power consumption with a single channel receiver, the total integrated noise in a multi-channel receiver is:
   a) worse
   b) better
   c) same
   d) It’s a flexible design parameter and can be made better if desired (correct)

   The correct answer is “d)” which was discussed in slide 20.

Post-test Questions

9.The same jitter robustness of a perfect multi-channel receiver can be achieved with practical finite order multi-channel filter-bank receivers?

a) False (correct)
b) True

The correct answer is “a)”, it is not exactly the same but it is very close as shown throughout the course.

10. Why is the LMS initialization important in the background calibration algorithm?

a) To achieve faster convergence
b) To achieve a cleaner convergence
c) To improve the steady state error
d) a and b are both correct (correct)

The correct answer is “d)”, slide 27 illustrates this point.

Glossary

- Multi-channel: Collection of multiple channels or paths connected in a particular topology, typically connected in parallel.
- Filter-bank: Parallel connection of filters driven by a common input signal.
- Brickwall filter: Ideal filter whose frequency response resembles a brickwall.
- Analog filter: Filter whose input and output signals are analog, i.e. continuous-time.
- Sinc filter: Discrete-time filter based on time windowing whose frequency response is a sinc response.
- Time-Interleaved: Topology based on time multiplexing that uses uniformly spaced phases in a clock period to sampled a signal at a fraction of Nyquist rate.
- Clock-Jitter: Clock timing uncertainty.
- Digital Background Calibration: Calibration performed at the digital back-end of a system.

The End

Thank you

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Related Publications

Zhuizhuan Yu, Jun Zhou, Mario Ramirez, Sebastian Hoyos, Brian M. Sadler**, "The impact of ADC nonlinearity in a mixed-signal compressive sensing system for frequency-domain sparse signals,"** *Physical Communication*, 17 November 2011, ISSN 1874-4907, 10.1016/j.phycom.2011.10.007.

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Thanks!